intel MCS-4 MICRO COMPUTER SET

NOVEMBER 1971

- Microprogrammable General Purpose Computer Set
- 4-Bit Parallel CPU With 45 Instructions
- Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching
- Binary and Decimal Arithmetic Modes
- Addition of Two 8-Digit Numbers in 850 Microseconds
- 2-Phase Dynamic Operation
- 10.8 Microsecond Instruction Cycle
- Easy Expansion – One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM
- Unlimited Number of Output Lines
- Single Power Supply Operation ($V_{DD} = -15$ Volts)
- Packaged in 16-Pin Dual In-Line Configuration

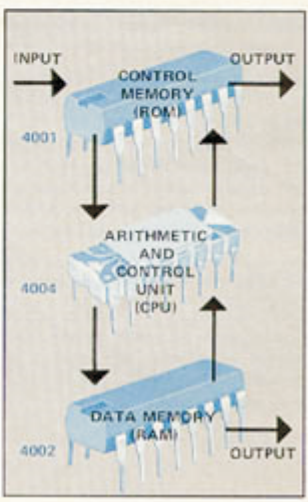
The MCS-4 is a microprogrammable computer set designed for applications such as test systems, peripherals, terminals, billing machines, measuring systems, numeric and process control. The 4004 CPU, 4003 SR, and 4002 RAM are standard building blocks. The 4001 ROM contains the custom microprogram and is implemented using a metal mask according to customer specifications.

MCS-4 systems interface easily with switches, keyboards, displays, teletypewriters, printers, readers, A-D converters and other popular peripherals.

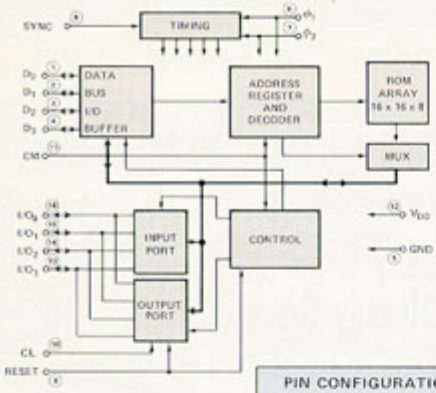
A system built with the MCS-4 micro computer set can have up to 4K x 8 bit ROM words, 1280 x 4 bit RAM characters and 128 I/O lines without requiring any interface logic. By adding a few simple gates the MCS-4 can have up to 48 RAM and ROM packages in any combination, and 192 I/O lines. The minimum system configuration consists of one CPU and one 256 x 8 bit ROM.

The MCS-4 has a very powerful instruction set that allows both binary and decimal arithmetic. It includes conditional branching, jump to subroutine, and provides for the efficient use of ROM look-up tables by indirect fetching.

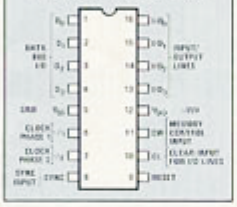
The Intel MCS-4 micro computer set (4001/2/3/4) is fabricated with Silicon Gate Technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.



4001 256 x 8 BIT MASK PROGRAMMABLE ROM AND 4 BIT I/O PORT



PIN CONFIGURATION



The 4001 is a 2048-bit metal mask programmable ROM providing custom microprogramming capability for the MCS-4 micro computer set. It is organized as 256 x 8 bit words.

Address and data are transferred in and out by time multiplexing on 4 data bus lines. Timing is internally generated using two clock signals, ϕ_1 and ϕ_2, and a SYNC signal supplied by the 4004. Addresses are received from the CPU on three time periods following SYNC, and select 1 out of 256 words and 1 out of 16 ROM's. For that purpose, each ROM is identified as #0, 1, 2, through 15, by metal option. A Command Line (CM) is also provided and its scope is to select a ROM bank (group of 16 ROM's).

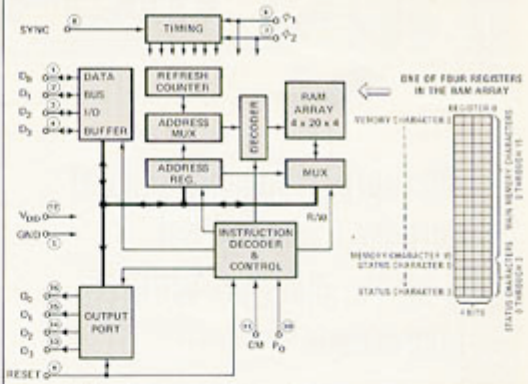
During the two time periods (M_1 & M_2) following the addressing time, information is transferred from the ROM to the data bus lines.

A second mode of operation of the ROM is as an Input/Output control device. In that mode a ROM chip will route information to and from data bus lines in and out of 4 I/O external lines. Each chip has the capability to identify itself for an I/O port operation, recognize an I/O port instruction and decide whether it is an Input or an Output operation and execute the instruction. An external signal (CL) will asynchronously clear the output register during normal operation.

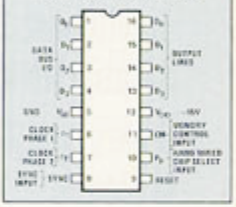
All internal flip flops (including the output register) will be reset when the RESET line goes low (negative voltage).

Each I/O pin can be uniquely chosen as either an input or output port by metal option. Direct or inverted input or output is optional. An on-chip resistor at the input pins, connected to either V_{DD} or V_{SS} is also optional. (See ordering information on page 12).

4002 320 BIT RAM AND 4 BIT OUTPUT PORT



PIN CONFIGURATION



The 4002 performs two functions. As a RAM it stores 320 bits arranged in 4 registers of twenty 4-bit characters each (16 main memory characters and 4 status characters). As a vehicle of communication with peripheral devices, it is provided with 4 output lines and associated control logic to perform output operations.

In the RAM mode, the operation is as follows: When the CPU executes an SRC instruction (see Instruction Set on page 5) it will send out the contents of the designated index register pair during X_2 and X_3 as an address to the RAM, and will activate one CM-RAM line at X_2 for the previously (Note 1) selected RAM bank (see Basic Instruction Cycle on page 5).

The data at X_2 and X_3 is interpreted as shown below:

X_2		X_3			
D_3 D_2	D_1 D_0	D_3	D_2	D_1	D_0
Chip # (0 through 3)	Register # (0 through 3)	Main Memory Character # (0 through 15)			

The status character locations (0 through 3) are selected by the OPA portion of one of the I/O and RAM Instructions.

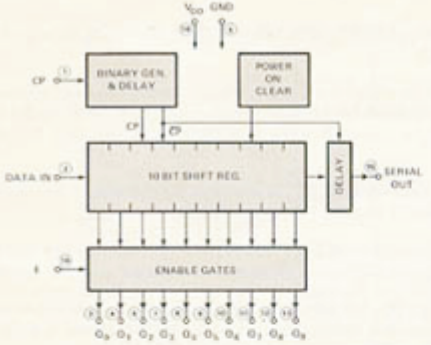
For chip selection, the 4002 is available in two metal options, 4002-1 and 4002-2. An external pin, P_0 (which may be hard wired to either V_{DD} or V_{SS}) is also available for chip selection. The chip number is assigned as follows:

Chip #	4002 Option	P_0	D_3	D_2 @ X_2
0	4002-1	GND	0	0
1	4002-1	V_{DD}	0	1
2	4002-2	GND	1	0
3	4002-2	V_{DD}	1	1

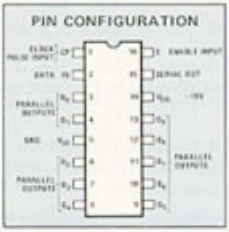
Timing is internally generated using two clock signals, ϕ_1 and ϕ_2, and a sync signal provided by the 4004. Internal refresh circuitry maintains data levels in the cells.

All communications with the system is through the data bus. The I/O port permits data out from the system. When the external RESET signal goes low, the memory and all static flip-flops (including the output registers) will be cleared. To fully clear the memory the RESET signal must be maintained for at least 32 memory cycles (32 x 8 clock periods).

4003 10 BIT SERIAL-IN/PARALLEL-OUT, SERIAL-OUT SHIFT REGISTER (SR)



PIN CONFIGURATION



The 4003 is a 10 bit static shift register with serial-in, parallel-out and serial-out data. Its function is to increase the number of output lines to interface with I/O devices such as keyboards, displays, printers, teletypewriters, switches, readers, A-D converters, etc.

Data is loaded serially and is available in parallel on 10 output lines which are accessed through enable logic. When enabled (E = low), the shift register contents is read out; when not enabled (E = high), the parallel-out lines are at V_{SS}. The serial-out line is not affected by the enable logic.

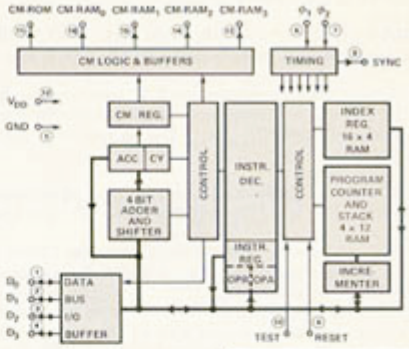
Data is also available serially permitting an indefinite number of similar devices to be cascaded together to provide shift register length multiples of 10.

The data shifting is controlled by the CP signal. An internal power-on-clear circuit will clear the shift register ($Q_i = V_{SS}$) between the application of the supply voltage and the first CP signal.

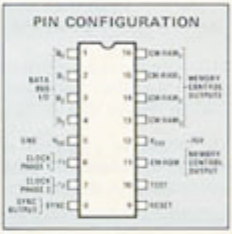
4002 320 BIT RAM AND 4 BIT OUTPUT PORT

NOTE 1: Bank switching is accomplished by the CPU after receiving a "DCL" (designate command line) instruction. Prior to execution of the DCL instruction the desired CM-RAM$_i$ code has been stored in the accumulator (for example through an LDM instruction). During DCL the CM-RAM$_i$ code is transferred from the accumulator to the CM-RAM register. The RAM bank is then selected starting with the next instruction.

4004 4 BIT CENTRAL PROCESSOR UNIT (CPU) WITH 45 INSTRUCTIONS



PIN CONFIGURATION



The 4004 is a central processor unit (CPU) designed to work in conjunction with the other members of the MCS-4 (4001, 4002, 4003) for microprogrammable computer applications.

The CPU chip consists of a 4 bit adder, a 64 bit (16 x 4) index register, a 48 bit (4 x 12) program counter and stack (nesting up to three levels if possible), an address incrementer, an 8 bit instruction register and decoder, and control logic. Information flows between the 4004 and the other chips through a 4-line data bus. One 4004 may be combined with up to 48 ROM (4001) and RAM (4002) chips in any combination.

A typical machine cycle starts with the CPU sending a synchronization signal (SYNC) to the ROM's and RAM's. Next, 12 bits of ROM address are sent to the data bus using three clock cycles (@ .75 MHz). The address is then incremented by one and stored in the program counter. The selected ROM sends back 8 bits of instruction or data during the following 2 clock cycles. This information is stored in two registers: OPR and OPA. The next three clock cycles are used to execute the instruction. (See Basic Instruction Cycle on page 5.)

The ROM bank is controlled by a command ROM control signal (CM-ROM) and up to four RAM banks are controlled by four command RAM control signals (CM-RAM$_0$, CM-RAM$_1$, CM-RAM$_2$, CM-RAM$_3$). Bank switching is accomplished by the execution of the DCL instruction (see Note 1 this page).

An input test signal (TEST) is used in conjunction with the jump on condition (JCN) instruction. An external RESET signal is used to clear all registers and flip-flops. To fully clear all registers, the RESET signal must be applied for at least 8 memory cycles (8 x 8 clock periods). After RESET the program will start from "0" step and CM-RAM$_0$ will be selected.

The instruction repertoire of the 4004 consists of:

(a) 16 machine instructions (5 of which are double length).

(b) 14 accumulator group instructions.

(c) 15 input/output & RAM instructions.

MCS-4 Operation

The detailed functional specifications describing the operation of the system, the instruction set, the activity of the CPU for each instruction and some programming and hardware examples are published separately and are available upon request. Following is a brief outline of the system operation.

The **MCS-4** uses a 10.8 μsec instruction cycle. The CPU (4004) generates a synchronizing signal (SYNC), indicating the start of an instruction cycle, and sends it to the ROM's (4001) and RAM's (4002).

Basic instruction execution requires 8 or 16 cycles of a 750 KHz clock. In a typical sequence, the CPU sends 12 bits of address to the ROM's in the first three cycles (A_1, A_2, A_3). The selected ROM chip sends back 8 bits of instruction (OPR, OPA) to the CPU in the next two cycles (M_1, M_2). The instruction is then interpreted and executed in the final three cycles (X_1, X_2, X_3). (See Figure 2.)

The CPU, RAM's and ROM's can be controlled by an external RESET line. While RESET is activated the contents of the registers and flip-flops are cleared. After RESET, the CPU will start from address 0 and CM-RAM_0 is selected.

The **MCS-4** can have up to 4K x 8 bit ROM words, 1280 x 4 bit RAM characters and 128 I/O lines, without requiring any interface logic. By adding a few simple gates, the **MCS-4** can have up to 48 RAM and ROM packages in any combination and 192 I/O lines.

The 4001, 4002, and 4004 are interconnected by a 4-line data bus (D_0, D_1, D_2, D_3), used for all information flow between the chips except for control signals sent by the CPU on 6 additional lines. The interconnection of the **MCS-4** system is shown in Figure 1. An expanded configuration is shown. The minimum system configuration consists of one CPU (4004) and one ROM (4001). Figure 2 shows the activity on the data bus during each clock period, and how a basic instruction cycle is subdivided.

Each data bus output buffer has three possible states "1", "0", and floating. At a given time only one output buffer is allowed to drive a data line, therefore, all the other buffers must be in a floating condition. However, more than one input buffer per data line can receive data at the same time.

The **MCS-4** has a very powerful Instruction Set that allows both binary and decimal arithmetic. It includes conditional branching, jump to subroutine and provides for the efficient use of ROM look up tables by indirect fetching. Typically, two 8 digit numbers can be added in 850 μsec. The complete Instruction Set is shown on pages 5 and 6.

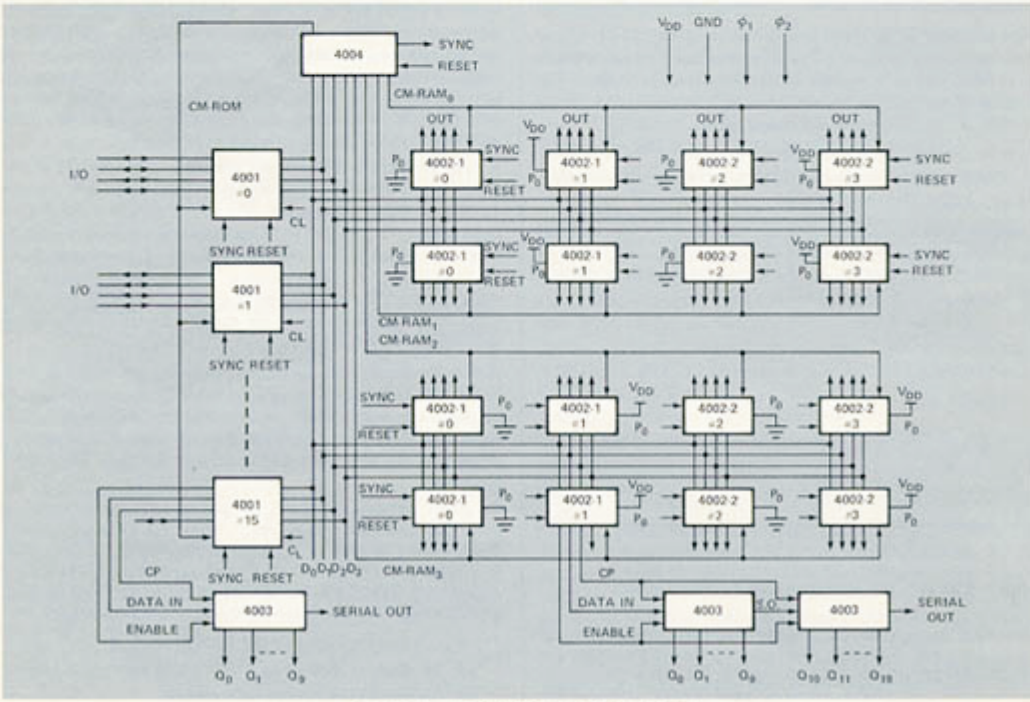
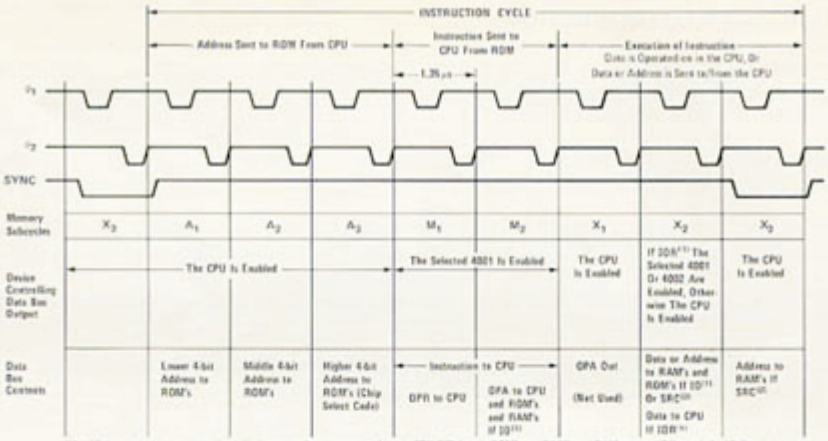


Figure 1. MCS-4 System Interconnection



(1) SD instructions control the flow of information between accumulator or CPU, I/O lines in ROM's and RAM's and RAM storage. SDR stands for SD Read. In this case the CPU will receive data from RAM storage locations or I/O input lines of 4001's.

(2) The SRC instruction designates the chip number and address for a following SD instruction.

Figure 2. MCS-4 Basic Instruction Cycle

Instruction Set

[Those instructions preceded by an asterisk (*) are 2 word instructions that occupy 2 successive locations in ROM]

MACHINE INSTRUCTIONS

MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
NOP	0 0 0 0	0 0 0 0	No operation.
*JCN	0 0 0 1 $A_2 A_2 A_2 A_2$	$C_1 C_2 C_3 C_4$ $A_1 A_1 A_1 A_1$	Jump to ROM address $A_2 A_2 A_2 A_2, A_1 A_1 A_1 A_1$ (within the same ROM that contains this JCN instruction) if condition $C_1 C_2 C_3 C_4$[1] is true, otherwise skip (go to the next instruction in sequence).
*FIM	0 0 1 0 $D_2 D_2 D_2 D_2$	R R R 0 $D_1 D_1 D_1 D_1$	Fetch immediate (direct) from ROM Data D_2, D_1 to index register pair location RRR.[2]
SRC	0 0 1 0	R R R 1	Send the address (contents of index register pair RRR) to ROM and RAM at X_2 and X_3 time in the Instruction Cycle.
FIN	0 0 1 1	R R R 0	Fetch indirect from ROM. Send contents of index register pair location 0 out as an address. Data fetched is placed into register pair location RRR at A_1 and A_2 time in the Instruction Cycle.
JIN	0 0 1 1	R R R 1	Jump indirect. Send contents of register pair RRR out as an address at A_1 and A_2 time in the Instruction Cycle.
*JUN	0 1 0 0 $A_2 A_2 A_2 A_2$	$A_3 A_3 A_3 A_3$ $A_1 A_1 A_1 A_1$	Jump unconditional to ROM address A_3, A_2, A_1.
*JMS	0 1 0 1 $A_2 A_2 A_2 A_2$	$A_3 A_3 A_3 A_3$ $A_1 A_1 A_1 A_1$	Jump to subroutine ROM address A_3, A_2, A_1, save old address. (Up 1 level in stack.)
INC	0 1 1 0	R R R R	Increment contents of register RRRR.[3]
*ISZ	0 1 1 1 $A_2 A_2 A_2 A_2$	R R R R $A_1 A_1 A_1 A_1$	Increment contents of register RRRR. Go to ROM address A_2, A_1 (within the same ROM that contains this ISZ instruction) if result ≠0, otherwise skip (go to the next instruction in sequence).
ADD	1 0 0 0	R R R R	Add contents of register RRRR to accumulator with carry.
SUB	1 0 0 1	R R R R	Subtract contents of register RRRR to accumulator with borrow.
LD	1 0 1 1	R R R R	Load contents of register RRRR to accumulator.
XCH	1 0 1 1	R R R R	Exchange contents of index register RRRR and accumulator.
BBL	1 1 0 0	D D D D	Branch back (down 1 level in stack) and load data DDDD to accumulator.
LDM	1 1 0 1	D D D D	Load data DDDD to accumulator.

See Notes on Page 6.

Continued on page 6.

INPUT/OUTPUT AND RAM INSTRUCTIONS

(The RAM's and ROM's operated on in the I/O and RAM instructions have been previously selected by the last SRC instruction executed.)

MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
WRM	1 1 1 0	0 0 0 0	Write the contents of the accumulator into the previously selected RAM main memory character.
WMP	1 1 1 0	0 0 0 1	Write the contents of the accumulator into the previously selected RAM output port. (Output Lines)
WRR	1 1 1 0	0 0 1 0	Write the contents of the accumulator into the previously selected ROM output port. (I/O Lines)
WR0 [4]	1 1 1 0	0 1 0 0	Write the contents of the accumulator into the previously selected RAM status character 0.
WR1 [4]	1 1 1 0	0 1 0 1	Write the contents of the accumulator into the previously selected RAM status character 1.
WR2 [4]	1 1 1 0	0 1 1 0	Write the contents of the accumulator into the previously selected RAM status character 2.
WR3 [4]	1 1 1 0	0 1 1 1	Write the contents of the accumulator into the previously selected RAM status character 3.
SBM	1 1 1 0	1 0 0 0	Subtract the previously selected RAM main memory character from accumulator with borrow.
RDM	1 1 1 0	1 0 0 1	Read the previously selected RAM main memory character into the accumulator.
RDR	1 1 1 0	1 0 1 0	Read the contents of the previously selected ROM input port into the accumulator. (I/O Lines)
ADM	1 1 1 0	1 0 1 1	Add the previously selected RAM main memory character to accumulator with carry.
RD0 [4]	1 1 1 0	1 1 0 0	Read the previously selected RAM status character 0 into accumulator.
RD1 [4]	1 1 1 0	1 1 0 1	Read the previously selected RAM status character 1 into accumulator.
RD2 [4]	1 1 1 0	1 1 1 0	Read the previously selected RAM status character 2 into accumulator.
RD3 [4]	1 1 1 0	1 1 1 1	Read the previously selected RAM status character 3 into accumulator.

ACCUMULATOR GROUP INSTRUCTIONS

CLB	1 1 1 1	0 0 0 0	Clear both. (Accumulator and carry)
CLC	1 1 1 1	0 0 0 1	Clear carry.
IAC	1 1 1 1	0 0 1 0	Increment accumulator.
CMC	1 1 1 1	0 0 1 1	Complement carry.
CMA	1 1 1 1	0 1 0 0	Complement accumulator.
RAL	1 1 1 1	0 1 0 1	Rotate left. (Accumulator and carry)
RAR	1 1 1 1	0 1 1 0	Rotate right. (Accumulator and carry)
TCC	1 1 1 1	0 1 1 1	Transmit carry to accumulator and clear carry.
DAC	1 1 1 1	1 0 0 0	Decrement accumulator.
TCS	1 1 1 1	1 0 0 1	Transfer carry subtract and clear carry.
STC	1 1 1 1	1 0 1 0	Set carry.
DAA	1 1 1 1	1 0 1 1	Decimal adjust accumulator.
KBP	1 1 1 1	1 1 0 0	Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.
DCL	1 1 1 1	1 1 0 1	Designate command line. (See note 1 on page 3.)

NOTES: [1] The condition code is assigned as follows:

$C_1 = 1$ Invert jump condition
$C_1 = 0$ Not invert jump condition
$C_2 = 1$ Jump if accumulator is zero
$C_3 = 1$ Jump if carry/link is a 1
$C_4 = 1$ Jump if test signal is a 0

[2] RRR is the address of 1 of 8 index register pairs in the CPU.

[3] RRRR is the address of 1 of 16 index registers in the CPU.

[4] Each RAM chip has 4 registers, each with twenty 4-bit characters subdivided into 16 main memory characters and 4 status characters. Chip number, RAM register and main memory character are addressed by an SRC instruction. For the selected chip and register, however, status character locations are selected by the instruction code (OPA).

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−55°C to +150°C
Input Voltages and Supply Voltage With Respect to V_{SS}	+0.5 to −20V
Power Dissipation	1.0 W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

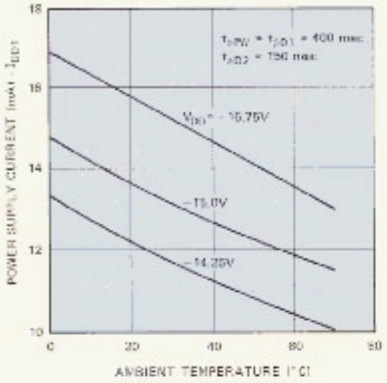
T_A = 0°C to +70°C; V_{DD} = −15V ±5%, V_{SS} = GND, $t_{\phi PW} = t_{\phi D1}$ = 400 nsec, $t_{\phi D2}$ = 150 nsec, unless otherwise specified
Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}). Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL})

PRODUCT	SYMBOL	PARAMETER	LIMIT MIN.	LIMIT TYP.[1]	LIMIT MAX.	UNIT	TEST CONDITIONS
SUPPLY CURRENT							
4001	I_{DD1}	AVERAGE SUPPLY CURRENT		15	30	mA	T_A = 25°C
4002	I_{DD2}	AVERAGE SUPPLY CURRENT		17	33	mA	T_A = 25°C
4003	I_{DD3}	AVERAGE SUPPLY CURRENT		5.0	8.5	mA	$t_{WL} = t_{WH}$ = 8 μsec; T_A = 25°C
4004	I_{DD4}	AVERAGE SUPPLY CURRENT		30	40	mA	T_A = 25°C
INPUT CHARACTERISTICS							
4001/2/3/4	I_{LI}	INPUT LEAKAGE CURRENT			10	μA	$V_{IL} = V_{DD}$
4001/2/3/4	V_{IH}	INPUT HIGH VOLTAGE (ALL INPUTS EXCEPT CLOCKS)	−1.5		+0.3	V	
4001/2/3/4	V_{IL}[2]	INPUT LOW VOLTAGE (ALL INPUTS EXCEPT CLOCKS)	V_{DD}		−5.5	V	
4001/2/4	V_{ILC}	CLOCK INPUT LOW VOLTAGE	V_{DD}		−13.4	V	
4001/2/4	V_{IHC}	CLOCK INPUT HIGH VOLTAGE	−1.5		+0.3	V	
4001	R_I	I/O PINS INPUT RESISTANCE	10	18	35	KΩ	Internal input resistor is optional
OUTPUT CHARACTERISTICS							
4001/2/4	I_{LO}	DATA BUS OUTPUT LEAKAGE CURRENT			10	μA	V_{OUT} = −12V, Chip disabled
4001/2/3/4	V_{OH}	OUTPUT HIGH VOLTAGE		0	−0.5	V	Driving 4000 Series loads only
4001/2/4	I_{OL1}	DATA LINES SINKING CURRENT "1" LEVEL	10	18		mA	V_{OUT} = 0V
4001/2	I_{OL2}	I/O OUTPUT LINES SINKING CURRENT, "1" LEVEL	2.5	5		mA	V_{OUT} = 0V
4003	I_{OL3}	PARALLEL OUT PINS SINKING CURRENT, "1" LEVEL	0.6	1.0		mA	V_{OUT} = 0V
4003	I_{OL4}	SERIAL OUT SINKING CURRENT, "1" LEVEL	1.0	2.0		mA	V_{OUT} = 0V
4004	I_{OL5}	CM-ROM SINKING CURRENT "1" LEVEL	6.5	12		mA	V_{OUT} = 0V
4004	I_{OL6}	CM-RAM LINES SINKING CURRENT "1" LEVEL	2.5	4		mA	V_{OUT} = 0V
4001/2/4	V_{OL1}	DATA LINES, CM LINES, SYNC OUTPUT LOW VOLTAGE	−12	−10	−6.5	V	I_{OL1} = 500 μA
4001/2	V_{OL2}	I/O OUTPUT LINES OUTPUT LOW VOLTAGE	−12	−7.5	−6.5	V	I_{OL2} = 50 μA
4003	V_{OL3}	OUTPUT LOW VOLTAGE	−11	−7.5	−6.5	V	I_{OL3} = 10 μA
4001/2/4	R_{OH1}	OUTPUT RESISTANCE DATA LINES "0" LEVEL		150	250	Ω	V_{OUT} = −0.5V
4001/2	R_{OH2}	OUTPUT RESISTANCE I/O LINES "0" LEVEL		1.2	1.8	KΩ	V_{OUT} = −0.5V
4003	R_{OH3}	PARALLEL-OUT PINS OUTPUT RESISTANCE "0" LEVEL		400	750	Ω	V_{OUT} = −0.5V
4003	R_{OH4}	SERIAL OUT OUTPUT RESISTANCE "0" LEVEL		650	1200	Ω	V_{OUT} = −0.5V
4004	R_{OH5}	CM-ROM OUTPUT RESISTANCE "0" LEVEL		320	600	Ω	V_{OUT} = −0.5V
4004	R_{OH6}	CM-RAM LINES OUTPUT RESISTANCE "0" LEVEL		1.1	1.8	KΩ	V_{OUT} = −0.5V

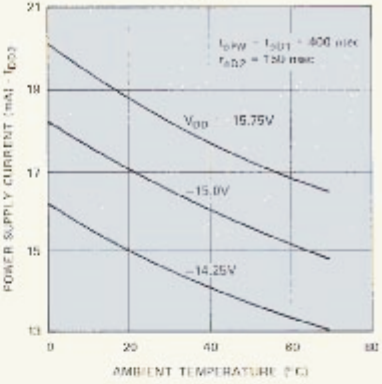
(1) Typical values are for T_A = 25°C and Nominal Supply Voltages.
(2) If non-inverting input option is used, V_{IL} = −6.5 Volts maximum.

Typical D.C. Characteristics

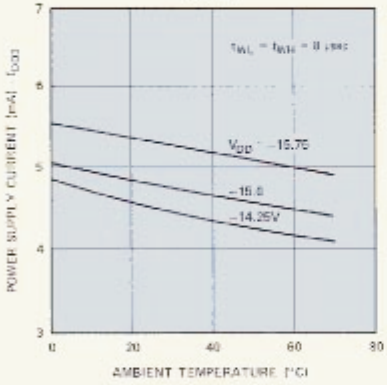
POWER SUPPLY CURRENT VS. TEMPERATURE (4001)



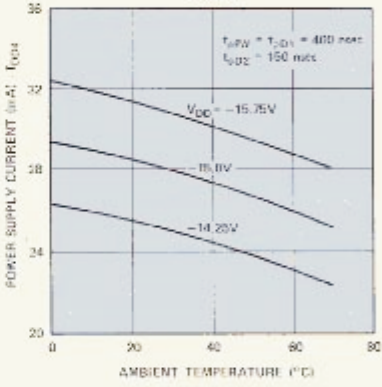
POWER SUPPLY CURRENT VS. TEMPERATURE (4002)



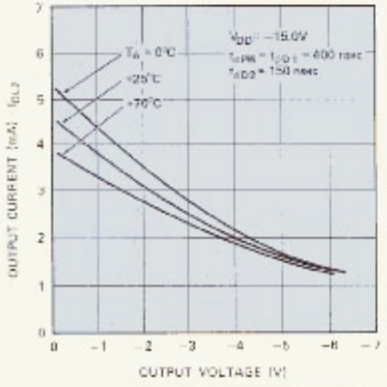
POWER SUPPLY CURRENT VS. TEMPERATURE (4003)



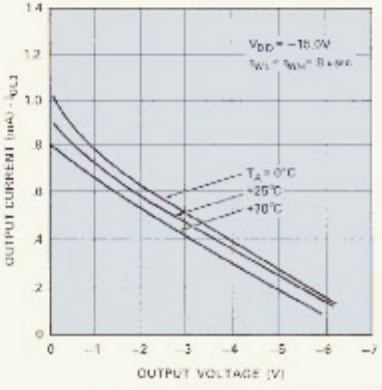
POWER SUPPLY CURRENT VS. TEMPERATURE (4004)



OUTPUT CURRENT VS. OUTPUT VOLTAGE (4001, 4002)



OUTPUT CURRENT VS. OUTPUT VOLTAGE (4003)



4001, 4002, 4004 A.C. Characteristics

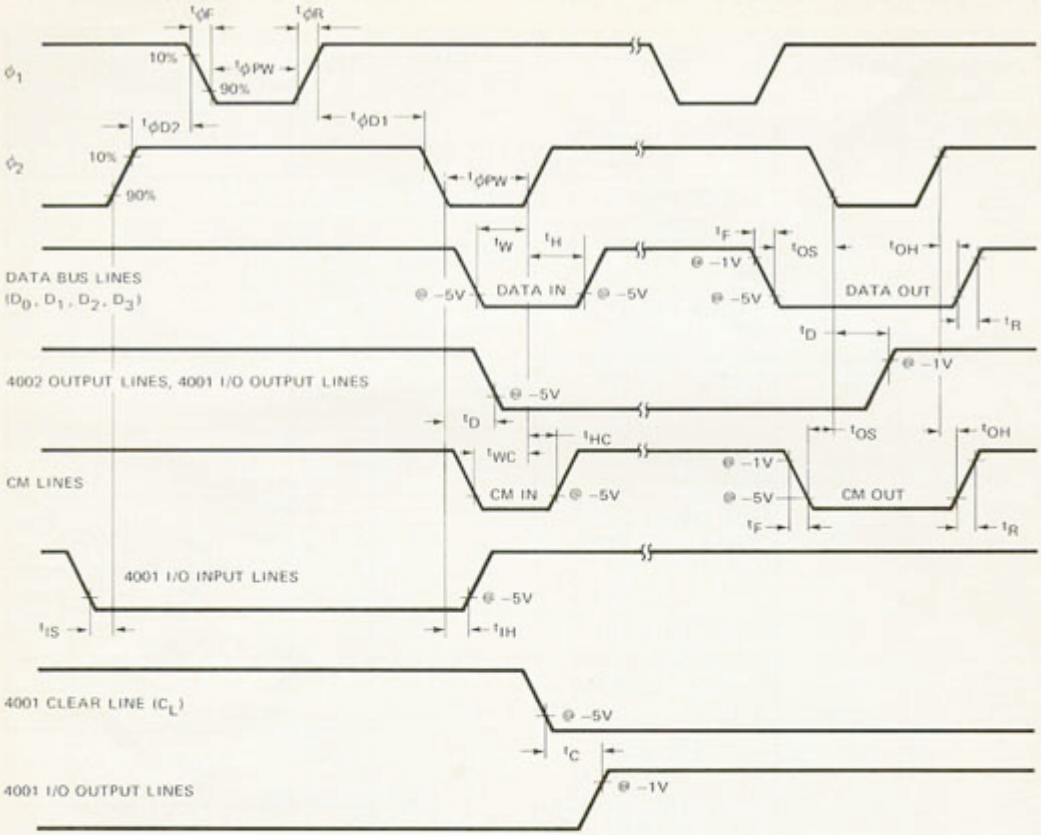
$T_A = 0°C$ to $+70°C$; $V_{DD} = -15V \pm 5\%$, $V_{SS} = GND$

PRODUCT	SYMBOL	TEST	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
4001/2/4	$t_{\phi R}$ $t_{\phi F}$	CLOCK RISE AND FALL TIMES	10	50	nsec	
	$t_{\phi PW}$	CLOCK WIDTH	380	480	nsec	
	$t_{\phi D1}$	CLOCK DELAY FROM ϕ_1 TO ϕ_2	400	550	nsec	
	$t_{\phi D2}$	CLOCK DELAY FROM ϕ_2 TO ϕ_1	150	300	nsec	
	t_W	DATA-IN WRITE TIME	350		nsec	
	t_H	DATA-IN HOLD TIME	40		nsec	
	t_{OS} [1]	SET TIME FOR DATA OUT, SYNC, CM-ROM, [2] CM-RAM$_i$ [2] LINES	0		nsec	C_{OUT} = 500 pF for data lines 500 pF for SYNC 160 pF for CM-ROM 50 pF for CM-RAM
	t_{OH}	HOLD TIME FOR DATA OUT, SYNC, CM-ROM, CM-RAM$_i$ LINES	50		nsec	C_{OUT} = 20 pF
	t_R, t_F	RISE AND FALL TIMES FOR DATA OUT, SYNC, CM-ROM, CM-RAM$_i$ LINES		500	nsec	C_{OUT} = 500 pF for data lines 500 pF for SYNC 160 pF for CM-ROM 50 pF for CM-RAM
4001/2	t_D	I/O OUTPUT LINES DELAY		600	nsec	C_{OUT} = 20 pF
	t_{WC}	CM WRITE TIME	350		nsec	
	t_{HC}	CM HOLD TIME	10		nsec	
4001	t_{IS}	I/O INPUT LINES SET TIME	50		nsec	
	t_{IH}	I/O INPUT LINES HOLD TIME	100		nsec	
	t_C [3]	I/O OUTPUT LINES DELAY ON CLEAR		200	nsec	C_{OUT} = 20 pF

NOTES: [1] Data out, SYNC, CM-ROM, and CM-RAM$_i$ lines are clocked out with the trailing edge of the ϕ_2 block.
[2] The CM-ROM and the selected CM-RAM$_i$ lines are always activated during A_3 time. They are also activated during M_2 time if an I/O and RAM instruction was fetched by the CPU, and during X_2 time if an SRC instruction was fetched by the CPU.
[3] Pin C_L on 4001 is used to asynchronously clear the output flip-flops associated with the I/O lines.

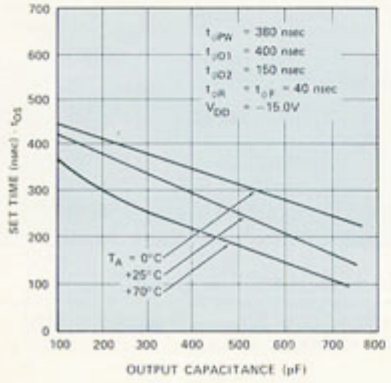
4001, 4002, 4004 Timing Diagram

Outputs with loading conditions specified on A.C. Characteristics table.

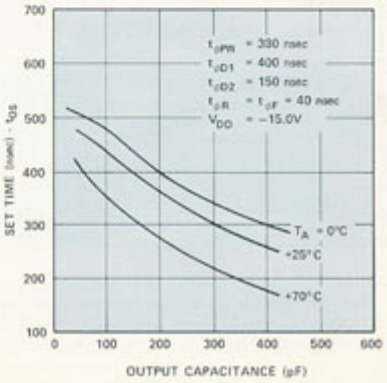


Typical Load Characteristics

SET TIME VS. OUTPUT CAPACITANCE
(DATA LINES FOR 4001, 4002, 4004
& SYNC FOR 4004)



SET TIME VS. OUTPUT CAPACITANCE
(CM-ROM 4004)



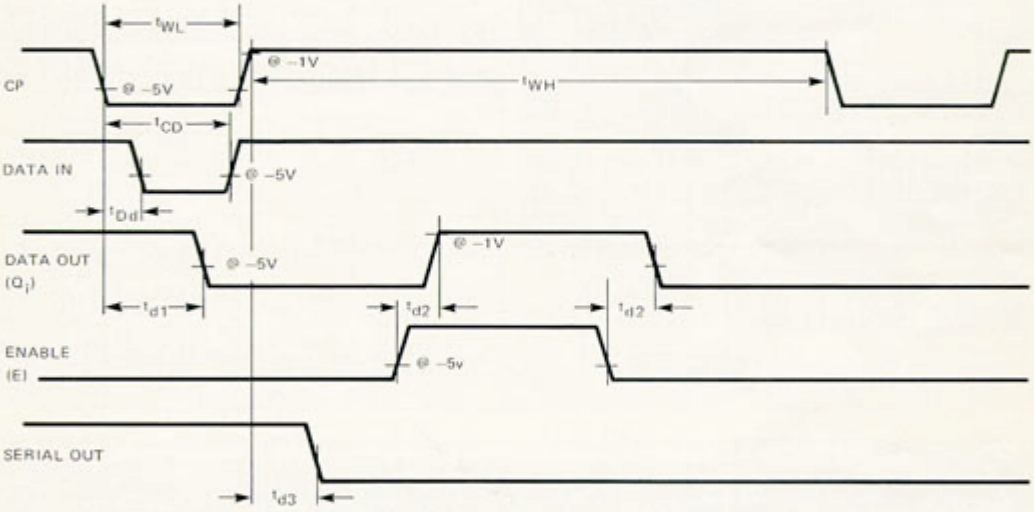
4003 A.C. Characteristics

T_A = 0°C to +70°C; V_{DD} = −15 ± 5%, V_{SS} = GND

SYMBOL	TEST	LIMIT		UNIT	CONDITIONS
		MIN.	MAX.		
t_{WL}	CP LOW WIDTH	6	10,000	μsec	
t_{WH}	CP HIGH WIDTH	6	Note (1)	μsec	
t_{CD}	CLOCK-ON TO DATA-OFF TIME	3		μsec	
t_{Dd}	CP TO DATA SET DELAY	Note (2)	250	nsec	
t_{d1}	CP TO DATA OUT DELAY	250	1,750	nsec	
t_{d2}	ENABLE TO DATA OUT DELAY		350	nsec	C_{OUT} = 20 pF
t_{d3}	CP TO SERIAL OUT DELAY	200	1,250	nsec	C_{OUT} = 20 pF

NOTES: (1) t_{WH} can be any time greater than 6 μsec.
(2) Data can occur prior to CP.

4003 Timing Diagram



Capacitance

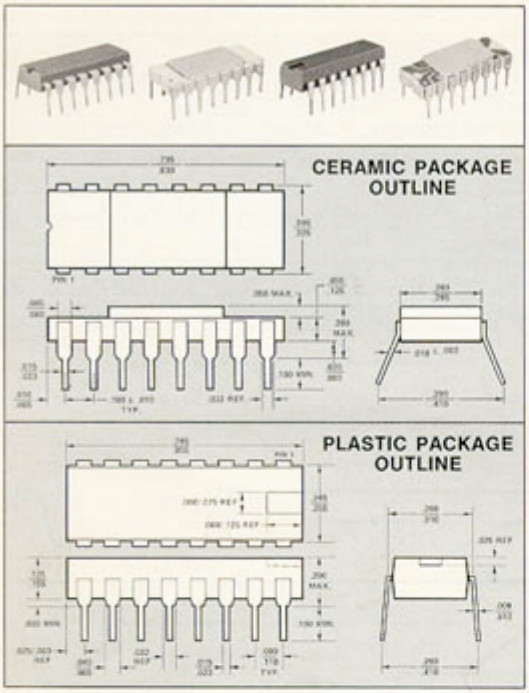
f = 1 MHz; V_{IN} = 0 V; T_A = 25° C ; Unmeasured Pins Grounded.

PRODUCT	SYMBOL	TEST	LIMIT (pF)	
			TYP.	MAX.
4001/2/3/4	C_{IN}	INPUT[1] CAPACITANCE	5	10
4001/2	$C_{\phi 1}$	CLOCK INPUT CAPACITANCE	8	15
4004	$C_{\phi 2}$	CLOCK INPUT CAPACITANCE	14	20

PRODUCT	SYMBOL	TEST	LIMIT (pF)	
			TYP.	MAX.
4002/4	C_{D1}	DATA BUS I/O LINES CAPACITANCE	6.5	10
4001	C_{D2}	DATA BUS I/O LINES CAPACITANCE	9.5	15

NOTE: (1) Refers to all input pins except data bus I/O and ϕ_1 and ϕ_2.

Packaging Information



Ordering Information

(1) The 4004 (CPU) is available in ceramic only and should be ordered as C4004.

(2) The 4001 (ROM), 4002 (RAM) and 4003 (SR) are presently available off the shelf in plastic only. These devices can be ordered in ceramic on special request. Standard devices should be ordered as follows:

P4001	Plastic Package
P4002-1	(Metal Option #1)- Plastic Package
P4002-2	(Metal Option #2)- Plastic Package
P4003	Plastic Package

(3) **Mask Programming of the 4001**

The custom patterns, chip numbers and I/O options (including inverting and non-inverting inputs or outputs and on-chip resistor connected to either V_{DD} or V_{SS}) must be specified on a truth table for each 4001 ordered. Blank custom truth tables are available upon request from Intel.

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