



I8048/8748/8035L INDUSTRIAL TEMPERATURE RANGE SINGLE COMPONENT 8-BIT MICROCOMPUTER

- 8048 Mask Programmable ROM
 - 8648 One-Time Factory Programmable EPROM
 - 8748 User Programmable/Erasable EPROM
 - 8035/8035L External ROM or EPROM
 - - 40°C to + 85°C Operation
-
- 8-Bit CPU, ROM, RAM, I/O in Single Package
 - Interchangeable ROM and EPROM Versions
 - Single 5V Supply
 - 2.5 μ sec and 5.0 μ sec Cycle Versions: All instructions 1 or 2 Cycles
 - Over 90 Instructions: 70% Single Byte
 - 1K \times 8 ROM/EPROM
 - 64 \times 8 RAM
 - 27 I/O LINES
 - Interval Timer/Event Counter
 - Easily Expandable Memory and I/O
 - Compatible with 8080/8085 Series Peripherals
 - Single Level Interrupt

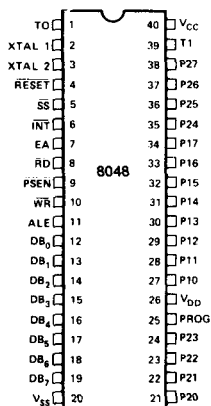
The Intel® 8048/8648/8748/8035 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

The 8048 contains a 1K \times 8 program memory, a 64 \times 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8035 is the equivalent of an 8048 without program memory. The 8035L has the RAM power-down mode of the 8048 while the 8035 does not. The 8648 is a one-time programmable (at the factory) 8748 which can be ordered as the first 25 pieces of a new 8048 ROM order. The substitution of 8648's for 8048's allows for very fast turnaround for initial code verification and evaluation units.

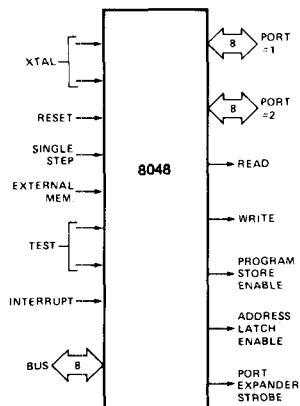
To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible versions of this single component microcomputer exist: the 8748 with user-programmable and erasable EPROM program memory for prototype and preproduction systems, the 8048 with factory-programmed mask ROM program memory for low cost, high volume production, and the 8035 without program memory for use with external program memories.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

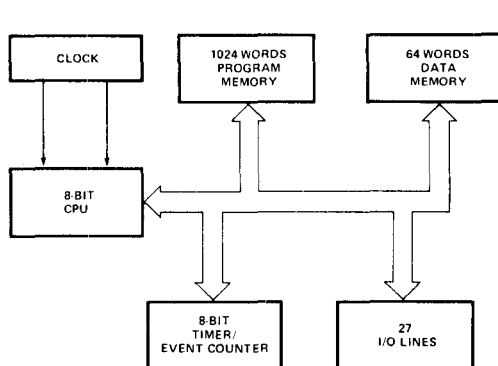
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTION

Designation	Pin #	Function	Designation	Pin #	Function
V _{SS}	20	Circuit GND potential	\overline{RD}	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)
V _{DD}	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 and 8035L.	\overline{RESET}	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low) (Non TTL V _{IH})
V _{CC}	40	Main power supply; +5V during operation and programming.	\overline{WR}	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.
PROG	25	Program pulse (+23V) input pin during 8748 programming.	ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.	PSEN	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.	\overline{SS}	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
DB ₀ -DB ₇ BUS	12-19	True bidirectional port which can be written or read synchronously using the \overline{RD} , \overline{WR} strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, \overline{RD} , and \overline{WR} .	EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
T0	1	Input pin testable using the conditional transfer instructions JTO and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction. T0 is also used during programming.	XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V _{IH})
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.	XTAL2	3	Other side of crystal input.
\overline{INT}	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)			

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle		Mnemonic	Description	Bytes	Cycles
Accumulator	ADD A, R	Add register to A	1	1	Subroutine	CALL addr	Jump to subroutine	2	2
	ADD A, @R	Add data memory to A	1	1		RET	Return	1	2
	ADD A, #data	Add immediate to A	2	2		RETR	Return and restore status	1	2
	ADDC A, R	Add register with carry	1	1	Flags	CLR C	Clear carry	1	1
	ADDC A, @R	Add data memory with carry	1	1		CPL C	Complement carry	1	1
	ADDC A, #data	Add immediate with carry	2	2		CLR F0	Clear flag 0	1	1
	ANL A, R	And register to A	1	1		CPL F0	Complement flag 0	1	1
	ANL A, @R	And data memory to A	1	1		CLR F1	Clear flag 1	1	1
	ANL A, #data	And immediate to A	2	2		CPL F1	Complement flag 1	1	1
	ORL A, R	Or register to A	1	1	Data Moves	MOV A, R	Move register to A	1	1
	ORL A, @R	Or data memory to A	1	1		MOV A, @R	Move data memory to A	1	1
	ORL A, #data	Or immediate to A	2	2		MOV A, #data	Move immediate to A	2	2
	XRL A, R	Exclusive or register to A	1	1		MOV R, A	Move A to register	1	1
	XRL A, @R	Exclusive or data memory to A	1	1		MOV @R, A	Move A to data memory	1	1
	XRL A, #data	Exclusive or immediate to A	2	2		MOV R, #data	Move immediate to register	2	2
	INC A	Increment A	1	1		MOV @R, #data	Move immediate to data memory	2	2
	DEC A	Decrement A	1	1		MOV A, PSW	Move PSW to A	1	1
	CLR A	Clear A	1	1		MOV PSW, A	Move A to PSW	1	1
	CPL A	Complement A	1	1		XCH A, R	Exchange A and register	1	1
	DA A	Decimal adjust A	1	1		XCHA, @R	Exchange A and data memory	1	1
	SWAP A	Swap nibbles of A	1	1		XCHD A, @R	Exchange nibble of A and register	1	1
Input/Output	RL A	Rotate A left	1	1		MOVX A, @R	Move external data memory to A	1	2
	RLC A	Rotate A left through carry	1	1	Timer/Counter	MOVX @R, A	Move A to external data memory	1	2
	RR A	Rotate A right	1	1		MOVP A, @A	Move to A from current page	1	2
	RRC A	Rotate A right through carry	1	1		MOV P3 A, @A	Move to A from page 3	1	2
	IN A, P	Input port to A	1	2		MOV A, T	Read timer/counter	1	1
	OUTL P, A	Output A to port	1	2		MOV T, A	Load timer/counter	1	1
	ANL P, #data	And immediate to port	2	2		STRT T	Start timer	1	1
	ORL P, #data	Or immediate to port	2	2		STRT CNT	Start counter	1	1
	INS A, BUS	Input BUS to A	1	2		STOP TCNT	Stop timer/counter	1	1
	OUTL BUS, A	Output A to BUS	1	2		EN TCNTI	Enable timer/counter interrupt	1	1
	ANL BUS, #data	And immediate to BUS	2	2		DIS TCNTI	Disable timer/counter interrupt	1	1
Registers	ORL BUS, #data	Or immediate to BUS	2	2	Control	EN I	Enable external interrupt	1	1
	MOVD A, P	Input expander port to A	1	2		DIS I	Disable external interrupt	1	1
	MOVD P, A	Output A to expander port	1	2		SEL RB0	Select register bank 0	1	1
	ANLD P, A	And A to expander port	1	2		SEL RB1	Select register bank 1	1	1
Branch	ORLD P, A	Or A to expander port	1	2		SEL MB0	Select memory bank 0	1	1
	INC R	Increment register	1	1		SEL MB1	Select memory bank 1	1	1
	INC @R	Increment data memory	1	1		ENT0 CLK	Enable clock output on T0	1	1
	DEC R	Decrement register	1	1		NOP	No operation	1	1
	JMP addr	Jump unconditional	2	2					
	JMP @A	Jump indirect	1	2					
	DJNZ R, addr	Decrement register and skip	2	2					
	JC addr	Jump on carry = 1	2	2					
	JNC addr	Jump on carry = 0	2	2					
	JZ addr	Jump on A zero	2	2					
	JNZ addr	Jump on A not zero	2	2					
	JT0 addr	Jump on T0 = 1	2	2					
	JNT0 addr	Jump on T0 = 0	2	2					
	JT1 addr	Jump on T1 = 1	2	2					
	JNT1 addr	Jump on T1 = 0	2	2					
	JF0 addr	Jump on F0 = 1	2	2					
	JF1 addr	Jump on F1 = 1	2	2					
	JTF addr	Jump on timer flag	2	2					
	JNI addr	Jump on INT = 0	2	2					
	JBb addr	Jump on accumulator bit	2	2					

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ABSOLUTE MAXIMUM RATINGS*

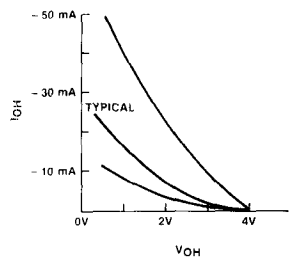
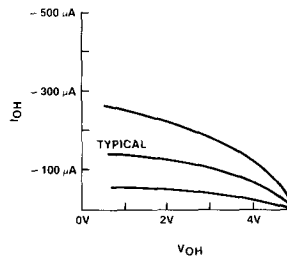
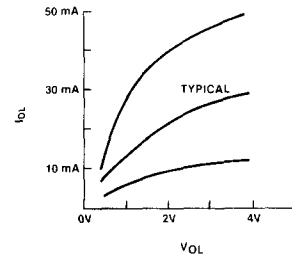
Ambient Temperature Under Bias . . . - 40°C to + 85°C
 Storage Temperature - 65°C to + 125°C
 Voltage On Any Pin With Respect
 to Ground - 0.5V to + 7V
 Power Dissipation 1.5 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS

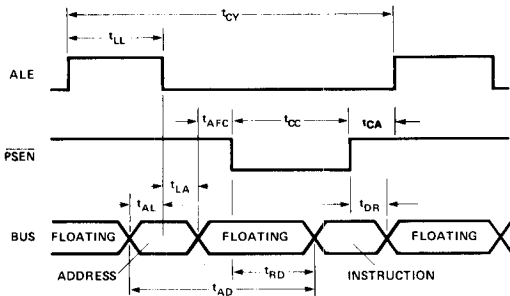
$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = V_{DD} = +5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All Except $\overline{\text{RESET}}$, XTAL1, XTAL2)	- 0.5		0.8	V	
V_{IL1}	Input Low Voltage ($\overline{\text{RESET}}$, X1, X2)	- 0.5		0.6	V	
V_{IH}	Input High Voltage (All Except XTAL1, XTAL 2, $\overline{\text{RESET}}$)	2.2		V_{CC}	V	
V_{IH1}	Input High Voltage (XTAL1, XTAL2, $\overline{\text{RESET}}$)	3.8		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE)			0.45	V	$I_{OL} = 1.6\text{ mA}$
V_{OL1}	Output Low Voltage (P10-P17, P20-P27)			0.45	V	$I_{OL} = 1.2\text{ mA}$
V_{OL2}	Output Low Voltage (All Other Outputs)			0.45	V	$I_{OL} = 0.8\text{ mA}$
V_{OH}	Output High Voltage (BUS)	2.4			V	$I_{OH} = -280\text{ }\mu\text{A}$
V_{OH1}	Output High Voltage ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{ALE}}$, $\overline{\text{PSEN}}$)	2.4			V	$I_{OH} = -80\text{ }\mu\text{A}$
V_{OH2}	Output High Voltage (All Other Outputs)	2.4			V	$I_{OH} = -30\text{ }\mu\text{A}$
I_{LI}	Input Leakage Current (T1, $\overline{\text{INT}}$)			± 10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{LI1}	Input Leakage Current (P10-P17, P20-P27, EA, $\overline{\text{SS}}$)			- 600	μA	$V_{SS} + .45 \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current (BUS, T0) (High Impedance State)			± 10	μA	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$
I_{DD}	V_{DD} Supply Current		10	20	mA	
$I_{DD} + I_{CC}$	Total Supply Current		75	145	mA	

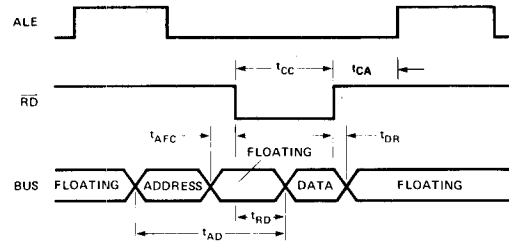
BUS**P1, P2****BUS, P1, P2**

WAVEFORMS

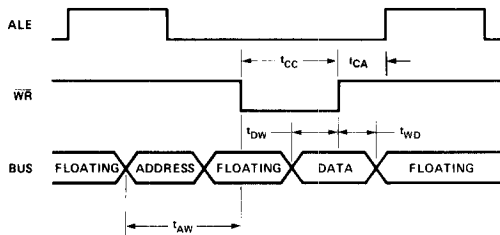
Instruction Fetch From External Program Memory



Read From External Data Memory



Write to External Data Memory



Input and Output Waveforms for A.C. Tests



A.C. CHARACTERISTICS

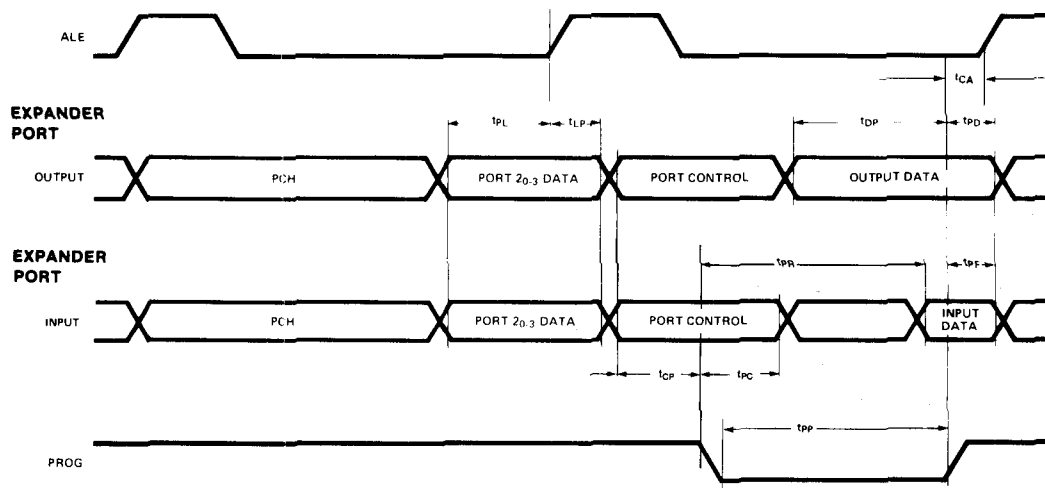
 $T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	8048/8035L		8748/8035		Unit	Conditions (Note 1)
		Min.	Max.	Min.	Max.		
t_{LL}	ALE Pulse Width	200		300		ns	
t_{AL}	Address Setup to ALE	120		120		ns	
t_{LA}	Address Hold from ALE	80		80		ns	
t_{CC}	Control Pulse Width ($\overline{\text{PSEN}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$)	400		600		ns	
t_{DW}	Data Setup Before $\overline{\text{WR}}$	420		600		ns	
t_{WD}	Data Hold After $\overline{\text{WR}}$	80		120		ns	$C_L = 20 \text{ pF}$
t_{CY}	Cycle Time	2.5	15.0	4.17	15.0	μs	(3.6 MHz XTAL 8748/8035)
t_{DR}	Data Hold	0	200	0	200	ns	
t_{RD}	$\overline{\text{PSEN}}$, $\overline{\text{RD}}$ to Data In		400		600	ns	
t_{AW}	Address Setup to $\overline{\text{WR}}$	230		260		ns	
t_{AD}	Address Setup to Data In		600		900	ns	
t_{AFC}	Address Float to $\overline{\text{RD}}$, $\overline{\text{PSEN}}$	-40		-60		ns	
t_{CA}	Control Pulse to ALE	10		10		ns	

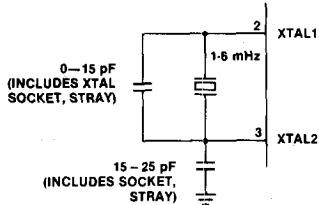
Note 1: Control Outputs: $C_L = 80 \text{ pF}$ $t_{CY} = 2.5 \mu\text{s}$ for 8048/8035L
 BUS Outputs: $C_L = 150 \text{ pF}$ 4.17 μs for 8748/8035

A.C. CHARACTERISTICS
 $T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CP}	Port Control Setup Before Falling Edge of PROG	115		ns	
t_{PC}	Port Control Hold After Falling Edge of PROG	65		ns	
t_{PR}	PROG to Time P2 Input Must Be Valid		860	ns	
t_{PF}	Input Data Hold Time	0	160	ns	
t_{DP}	Output Data Setup Time	230		ns	
t_{PD}	Output Data Hold Time	25		ns	
t_{PP}	PROG Pulse Width	920		ns	
t_{PL}	Port 2 I/O Data Setup	300		ns	
t_{LP}	Port 2 I/O Data Hold	120		ns	

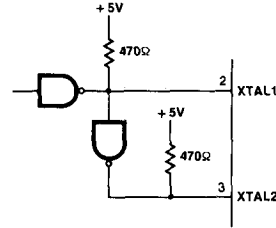
PORT 2 TIMING

CRYSTAL OSCILLATOR MODE



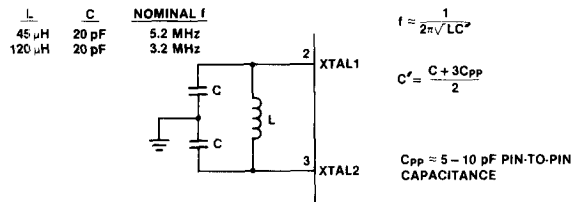
CRYSTAL SERIES RESISTANCE SHOULD BE <75Ω AT 6 MHz; <180Ω AT 3.6 MHz.

DRIVING FROM EXTERNAL SOURCE



BOTH X1 AND X2 SHOULD BE DRIVEN. RESISTORS TO V_{CC} ARE NEEDED TO ENSURE $V_{IH} = 3.8V$ IF TTL CIRCUITRY IS USED. THE MINIMUM HIGH AND THE MINIMUM LOW TIMES ARE 45%.

LC OSCILLATOR MODE



EACH C SHOULD BE APPROXIMATELY 20 pF, INCLUDING STRAY CAPACITANCE.

PROGRAMMING, VERIFYING, AND ERASING THE 8748 EPROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock Input (1 to 6 MHz)
RESET	Initialization and Address Latching
TEST 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input Data Output during Verify
P20-1	Address Input
V_{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING:

An attempt to program a mis-socketed 8748 will result in severe damage to the part. An indication of a properly socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify Sequence is:

1. $V_{DD} = 5V$, clock applied or internal oscillator operating, $\overline{\text{RESET}} = 0V$, TEST 0 = 5V, EA = 5V, BUS and PROG floating.
2. Insert 8748 in programming socket.
3. TEST 0 = 0V (select program mode).
4. EA = 23V (activate program mode).
5. Address applied to BUS and P20-1.
6. $\overline{\text{RESET}} = 5V$ (latch address).
7. Data applied to BUS.
8. $V_{DD} = 25V$ (programming power).
9. PROG = 0V followed by one 50 ms pulse to 23 V.
10. $V_{DD} = 5V$.
11. TEST 0 = 5V (verify mode).
12. Read and verify data on BUS.
13. TEST 0 = 0V.
14. $\overline{\text{RESET}} = 0V$ and repeat from step 5.
15. Programmer should be at conditions of step 1 when 8748 is removed from socket.

AC TIMING SPECIFICATION FOR PROGRAMMING

$T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{DD} = 25\text{V} \pm 1\text{V}$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	Address Setup Time to $\overline{\text{RESET}} \uparrow$	4tcy			
t_{WA}	Address Hold Time After $\overline{\text{RESET}} \uparrow$	4tcy			
t_{DW}	Data in Setup Time to $\text{PROG} \uparrow$	4tcy			
t_{WD}	Data in Hold Time After $\text{PROG} \downarrow$	4tcy			
t_{PH}	$\overline{\text{RESET}}$ Hold Time to Verify	4tcy			
t_{VDDW}	V_{DD}	4tcy			
t_{VDDH}	V_{DD} Hold Time After $\text{PROG} \downarrow$	0			
t_{PW}	Program Pulse Width	50	60	ms	
t_{TW}	Test 0 Setup Time for Program Mode	4tcy			
t_{WT}	Test 0 Hold Time After Program Mode	4tcy			
t_{DO}	Test 0 to Data Out Delay		4tcy		
t_{WW}	$\overline{\text{RESET}}$ Pulse Width to Latch Address	4tcy			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	2.0	μs	
t_{CY}	CPU Operation Cycle Time	5.0		μs	
t_{RE}	$\overline{\text{RESET}}$ Setup Time Before $\text{EA} \uparrow$	4tcy			

Note: If Test 0 is high too can be triggered by $\overline{\text{RESET}} \uparrow$

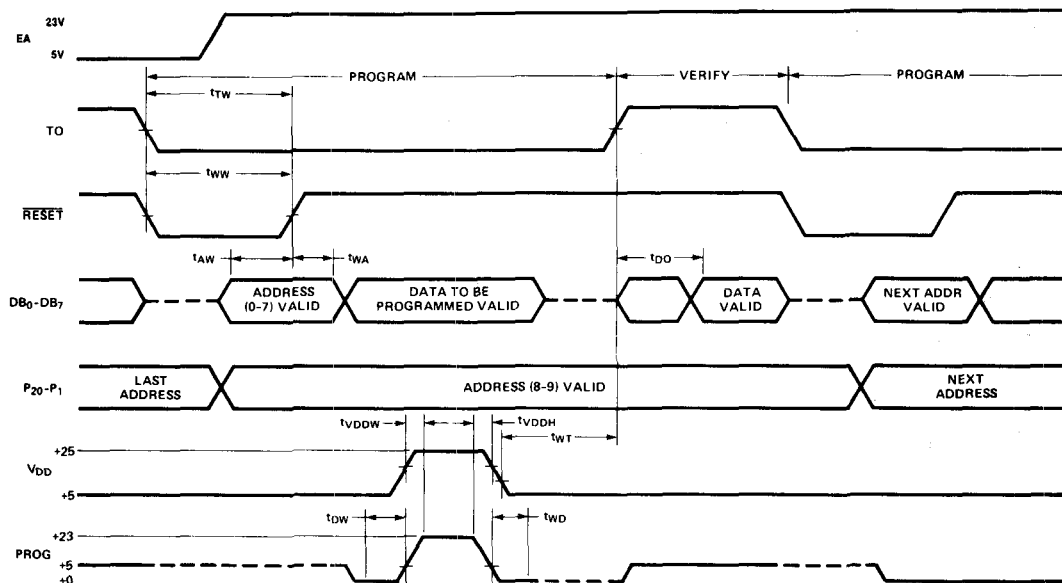
DC SPECIFICATION FOR PROGRAMMING

$T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{DD} = 25\text{V} \pm 1\text{V}$

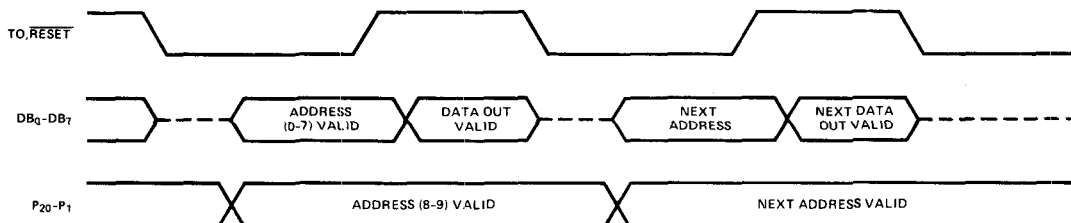
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DOH}	V_{DD} Program Voltage High Level	24.0	26.0	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	21.5	24.5	V	
V_{PL}	PROG Voltage Low Level		0.2	V	
V_{EAH}	EA Program or Verify Voltage High Level	21.5	24.5	V	8748
V_{EAH1}	EA1 Verify Voltage High Level	11.4	12.6	V	8048
V_{EAL}	EA Voltage Low Level		5.25	V	
I_{DD}	V_{DD} High Voltage Supply Current		30.0	mA	
I_{PROG}	PROG High Voltage Supply Current		16.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

WAVEFORMS FOR PROGRAMMING

COMBINATION PROGRAM/VERIFY MODE (EPROM'S ONLY)



VERIFY MODE (ROM/EPROM)



NOTES:

1. PROG MUST FLOAT IF EA IS LOW (i.e., $\neq 23V$), OR IF T0 = 5V FOR THE 8748. FOR THE 8048 PROG MUST ALWAYS FLOAT.
2. X1 AND X2 DRIVEN BY 3 MHz CLOCK WILL GIVE $5\mu\text{sec}$ t_{CY} . THIS IS ACCEPTABLE FOR .8 PARTS AS WELL AS STANDARD PARTS.

The 8748 EPROM can be programmed by either of two Intel products:

1. PROMPT-48 Microcomputer Design Aid, or
2. Universal PROM Programmer (UPP series) peripheral of the Intellec® Development System with a UPP-848 Personality Card.

Note: See the ROM/PROM section for 8048 ROM ordering procedures. To minimize turnaround time on the first 25 pieces 8648 may be specified on the ROM order.