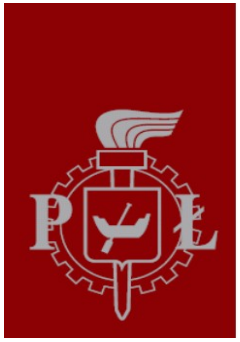


Politechnika Łódzka
Instytut Elektroniki

Programowanie Mikrokontrolerów

Architektura układu ATmega128(L), część 1.

mgr inż. Paweł Poryzała
Zakład Elektroniki Medycznej

Zagadnienia

- Charakterystyka układu ATmega128(L)
- Parametry elektryczne
- AVR CPU Core
  - ALU
  - Status Register
  - Register File
  - Stack Pointer
  - Memory Maps
  - Interrupts
- Schemat blokowy układu
- Clock Distribution
- Power Management
- Sysem Control And Reset
- GPIO i ich wykorzystanie

Krótka charakterystyka

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 133 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers + Peripheral Control Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 128K Bytes of In-System Self-programmable Flash program memory
  - 4K Bytes EEPROM
  - 4K Bytes Internal SRAM
  - Write/Erase cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C(1)
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Up to 64K Bytes Optional External Memory Space
  - Programming Lock for Software Security
  - SPI Interface for In-System Programming

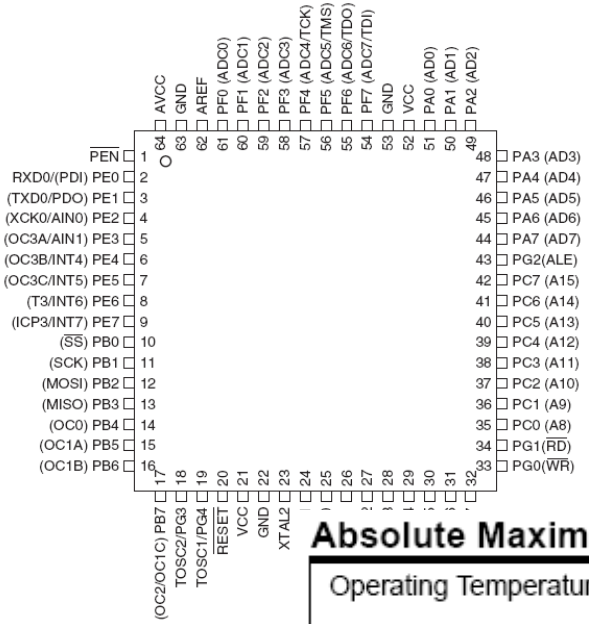
Krótka charakterystyka

- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - Two Expanded 16-bit Timer/Counters with Separate Prescaler, Compare Mode and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Two 8-bit PWM Channels
  - 6 PWM Channels with Programmable Resolution from 2 to 16 Bits
  - Output Compare Modulator
  - 8-channel, 10-bit ADC
    - 8 Single-ended Channels
    - 7 Differential Channels
    - 2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Dual Programmable Serial USARTs
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with On-chip Oscillator
  - On-chip Analog Comparator

Krótka charakterystyka

- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
  - Software Selectable Clock Frequency
  - ATmega103 Compatibility Mode Selected by a Fuse
  - Global Pull-up Disable
- I/O and Packages
  - 53 Programmable I/O Lines
  - 64-lead TQFP and 64-pad QFN/MLF
- Operating Voltages
  - 2.7 - 5.5V ATmega128L
  - 4.5 - 5.5V ATmega128
- Speed Grades
  - 0 - 8 MHz ATmega128L
  - 0 - 16 MHz ATmega128

Parametry elektryczne



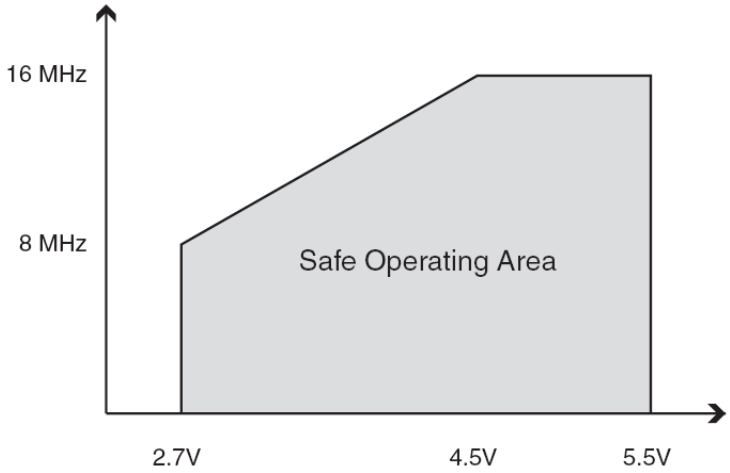
- Obudowa:
  - TQFP64
  - QFN64
- 53 programowalne linie IO

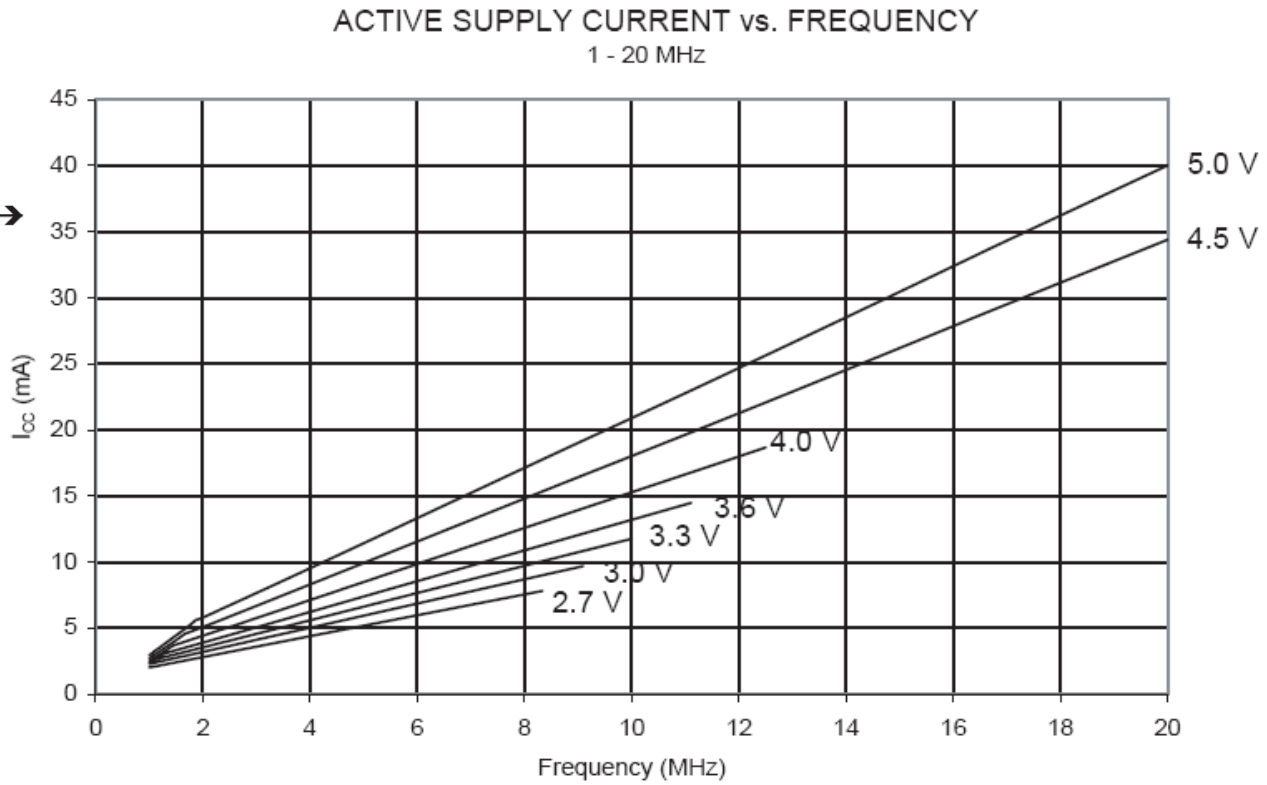
Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin except $\overline{\text{RESET}}$ with respect to Ground	-0.5V to V_{CC}+0.5V
Voltage on $\overline{\text{RESET}}$ with respect to Ground	-0.5V to +13.0V
Maximum Operating Voltage	6.0V
DC Current per I/O Pin	40.0 mA
DC Current V_{CC} and GND Pins	200.0 - 400.0mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

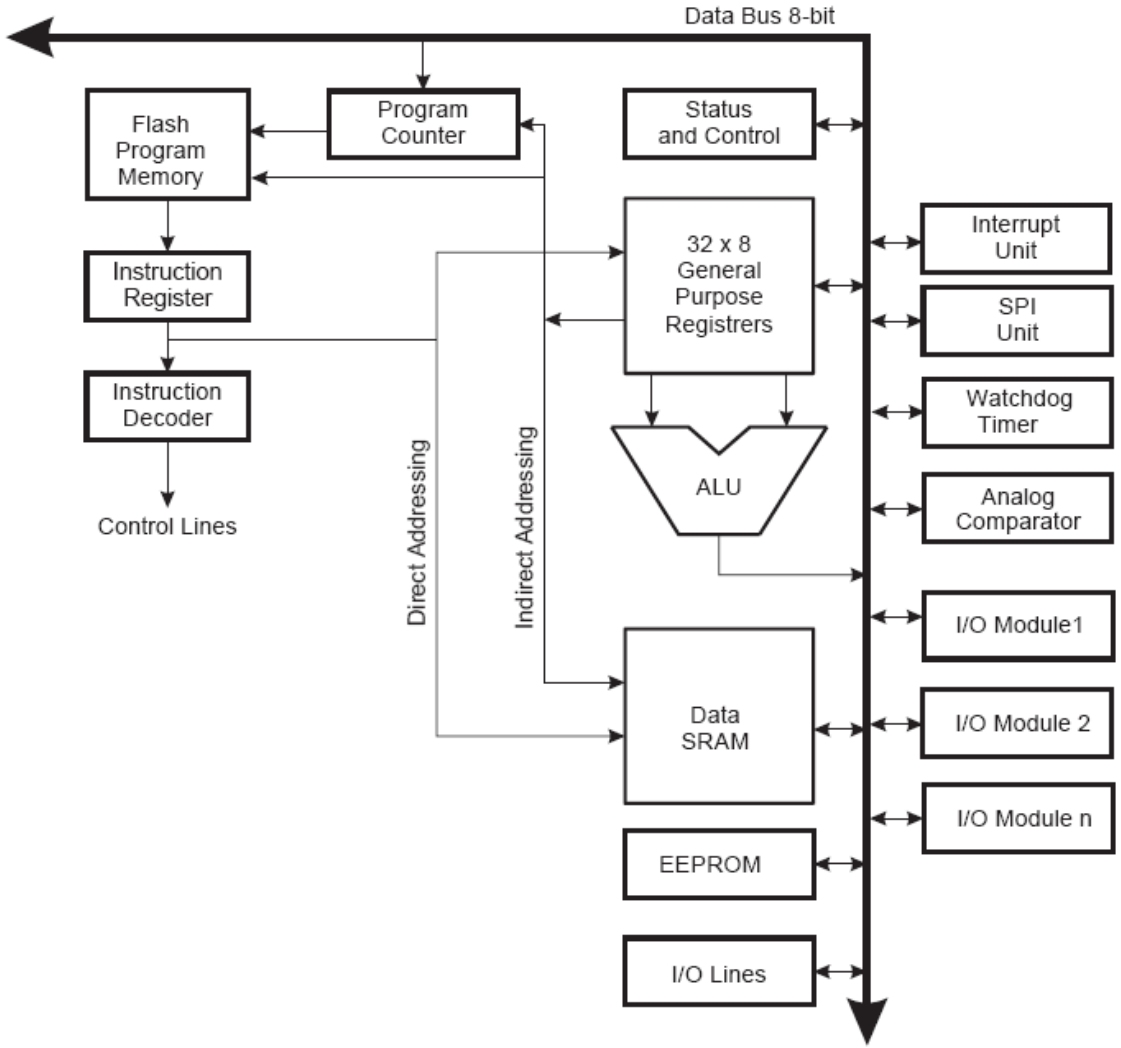
Parametry elektryczne





Jak długo będzie pracować ATmega128L (@7,3728MHz) zasilona z baterii CR2032 (3V, 220mAh)???

AVR CPU Core

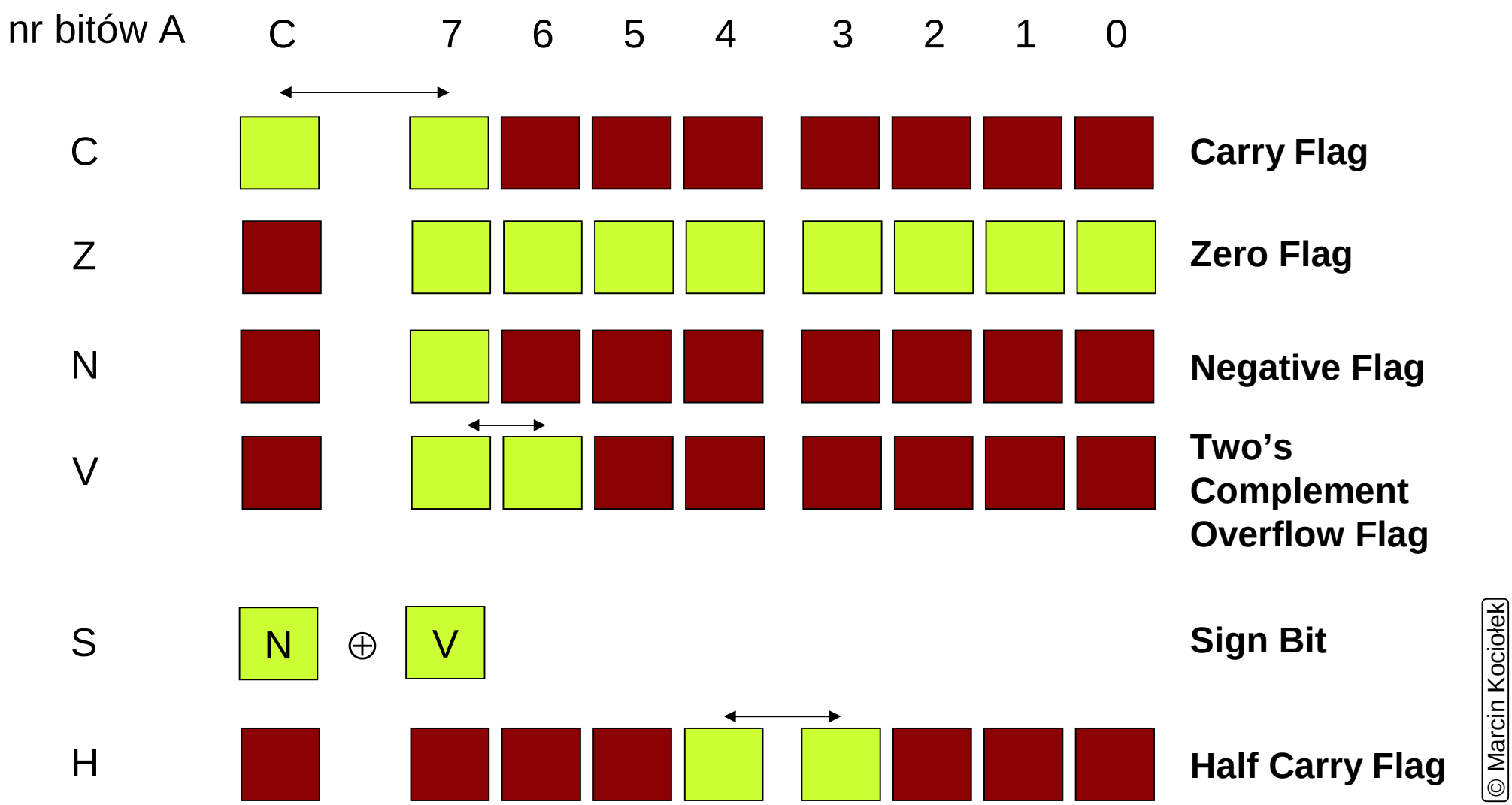

Data Bus 8-bit
Flash Program Memory
Program Counter
Status and Control
Instruction Register
Instruction Decoder
Control Lines
32 x 8 General Purpose Registrers
ALU
Direct Addressing
Indirect Addressing
Data SRAM
EEPROM
I/O Lines
Interrupt Unit
SPI Unit
Watchdog Timer
Analog Comparator
I/O Module1
I/O Module 2
I/O Module n

Status Register (SREG)

Bit	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

I: Global Interrupt Enable – globalne zezwolenie na przerwania
T: Copy Storage – bit tymczasowy
H: Half Carry Flag – flaga przeniesienia połówkowego
S: Sign Flag – flaga znaku
V: Overflow Flag – flaga przepełnienia (przepełnienie kodu U2)
N: Negative Flag – flaga wartości ujemnej
Z: Zero Flag – wskaźnik zera
C: Carry Flag – wskaźnik przeniesienia

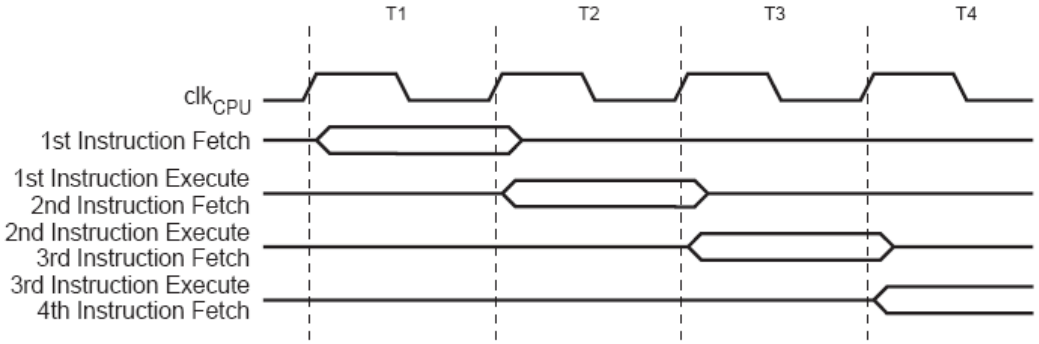
Znaczniki operacji ALU



© Marcin Kociołek

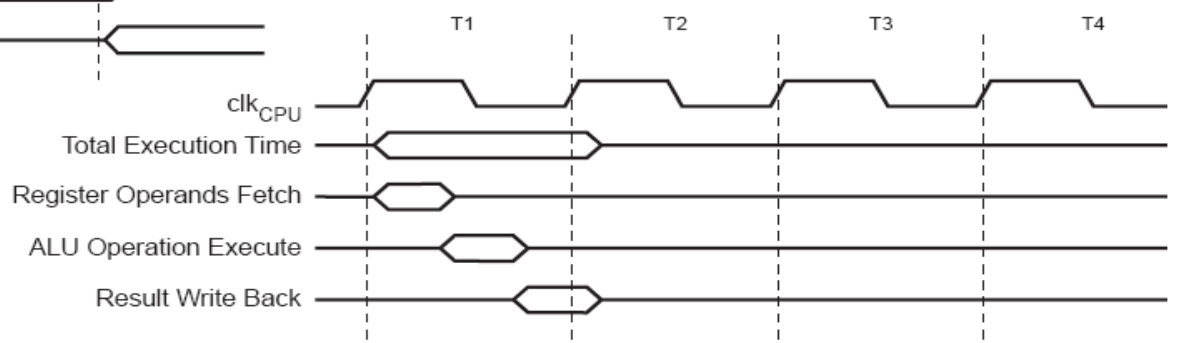
ALU

- Bezpośrednie połączenie z zestawem 32 rejestrów,
- Wykonuje operacje:
  - Arytmetyczne
  - Logiczne
  - Bitowe
- W przypadku ATmega128(L) rozszerzone o sprzętową mnożarkę (mnożenie ze znakiem oraz bez)

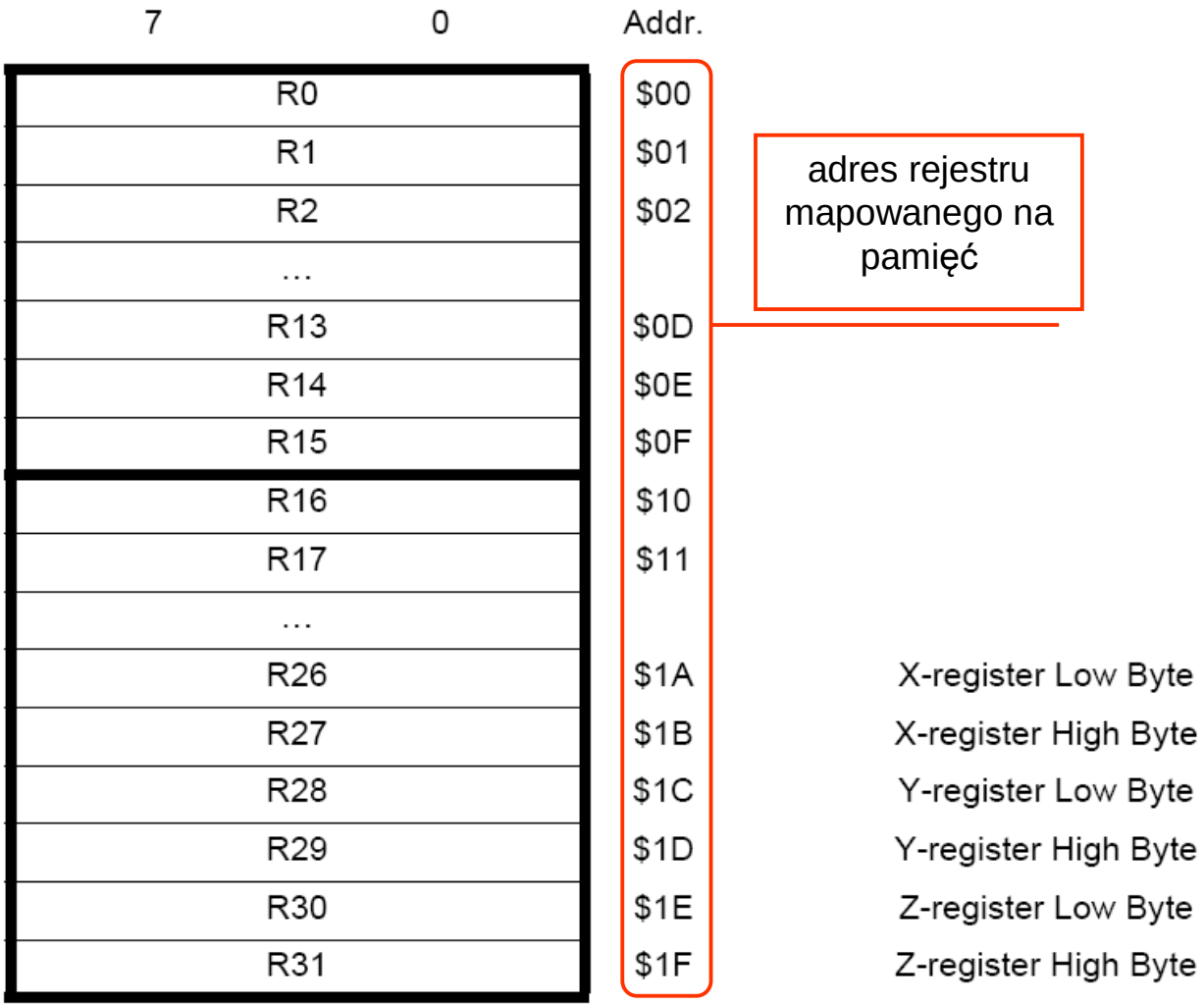


The Parallel Instruction Fetches and Instruction Executions

Single Cycle ALU Operation



Rejestry ogólnego przeznaczenia

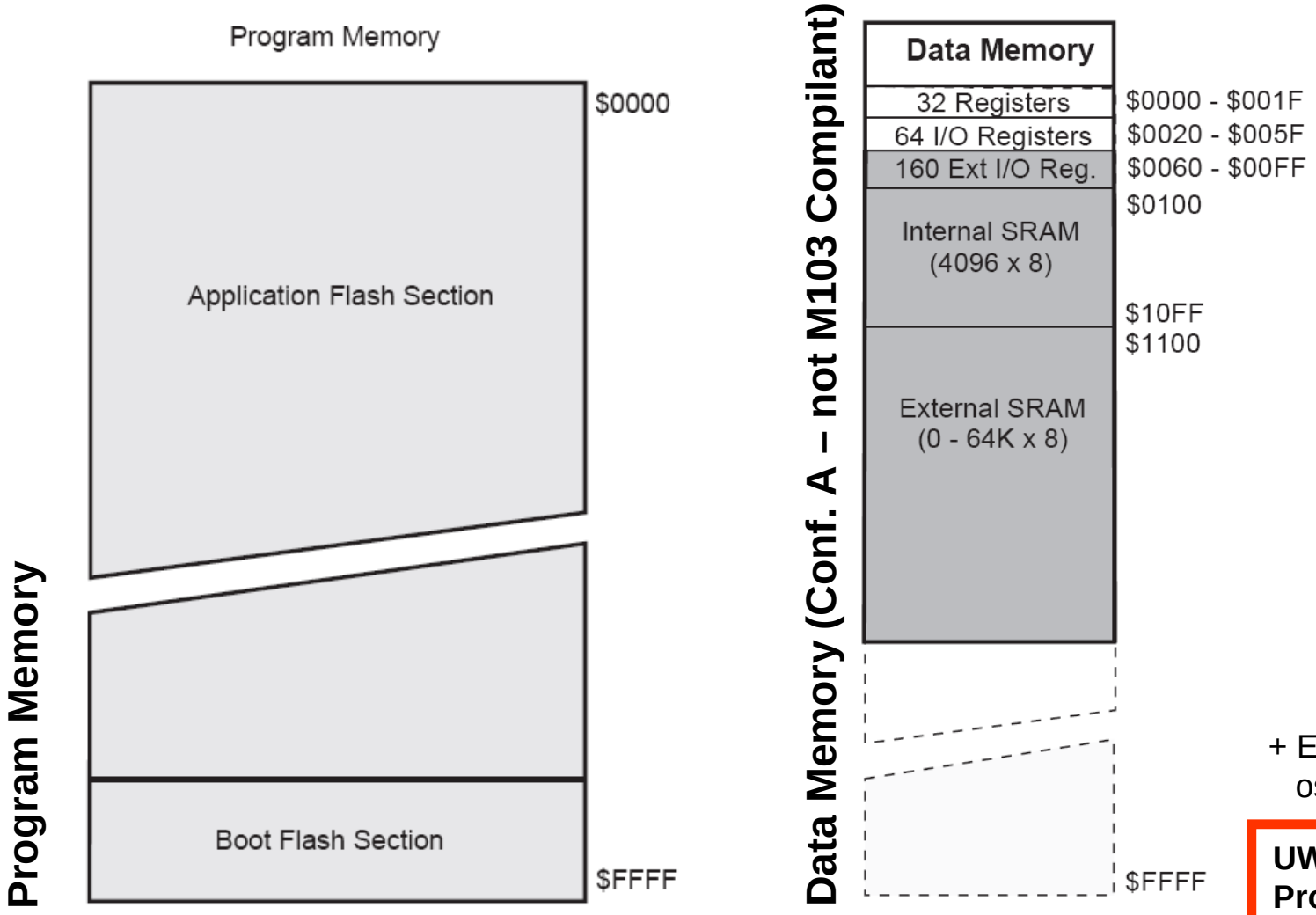


- Rejestry ogólnego przeznaczenia
- Rejestry adresowe X, Y oraz Z, automatyczna inkrementacja / dekrementacja

Stack Pointer

Bit	15	14	13	12	11	10	9	8
	SP15	**SP14**	**SP13**	**SP12**	**SP11**	**SP10**	**SP9**	**SP8**
	SP7	**SP6**	**SP5**	**SP4**	**SP3**	**SP2**	**SP1**	**SP0**
	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0

Mapy Pamięci

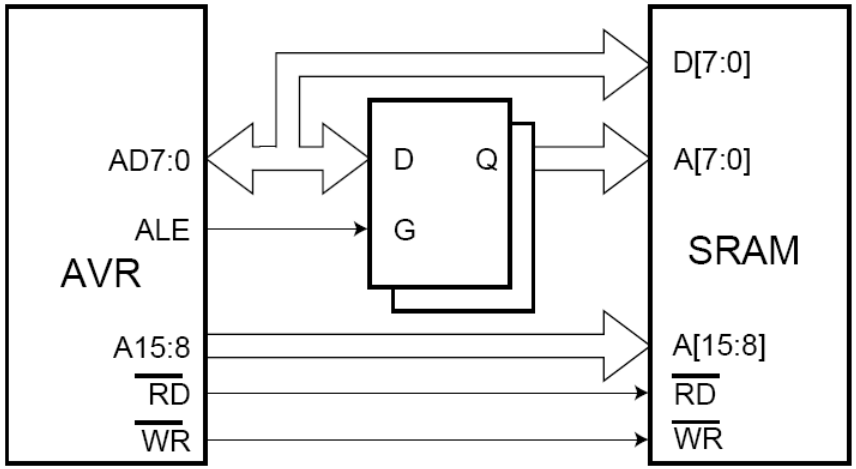


+ EEPROM obsługiwany jak osobny układ peryferyjny

UWAGA:
Problemy z bitem M103C!!!

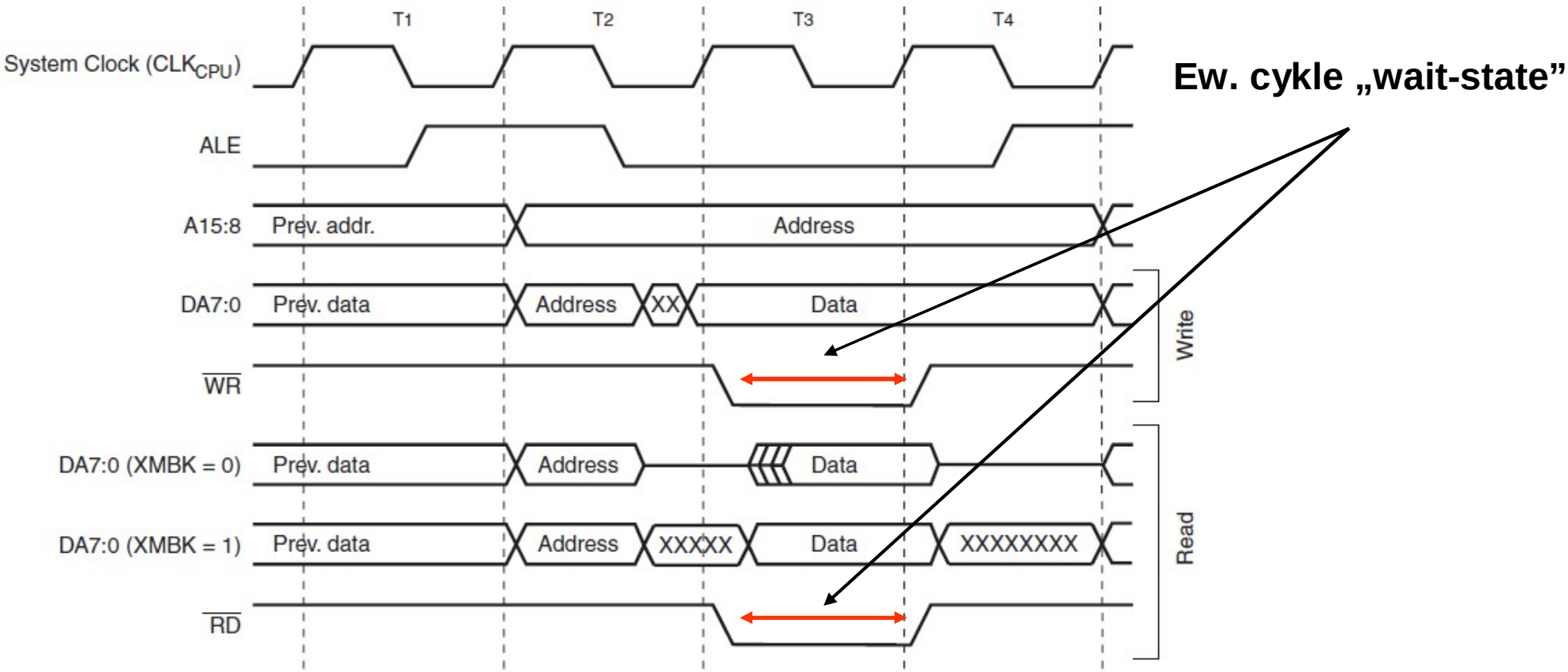
Interfejs pamięci zewnętrznej

- Interfejs do pamięci zewnętrznych SRAM lub Flash oraz peryferiów – LCD, przetworniki A/D, D/A
  - Możliwość konfiguracji dodatkowych cykli wait-state, niezależnie w różnych sektorach mapy adresowej,
  - Układy pull-up oraz bus-keeper na liniach adresowych oraz liniach danych – minimalizacja zużycia energii w stanach uśpienia.

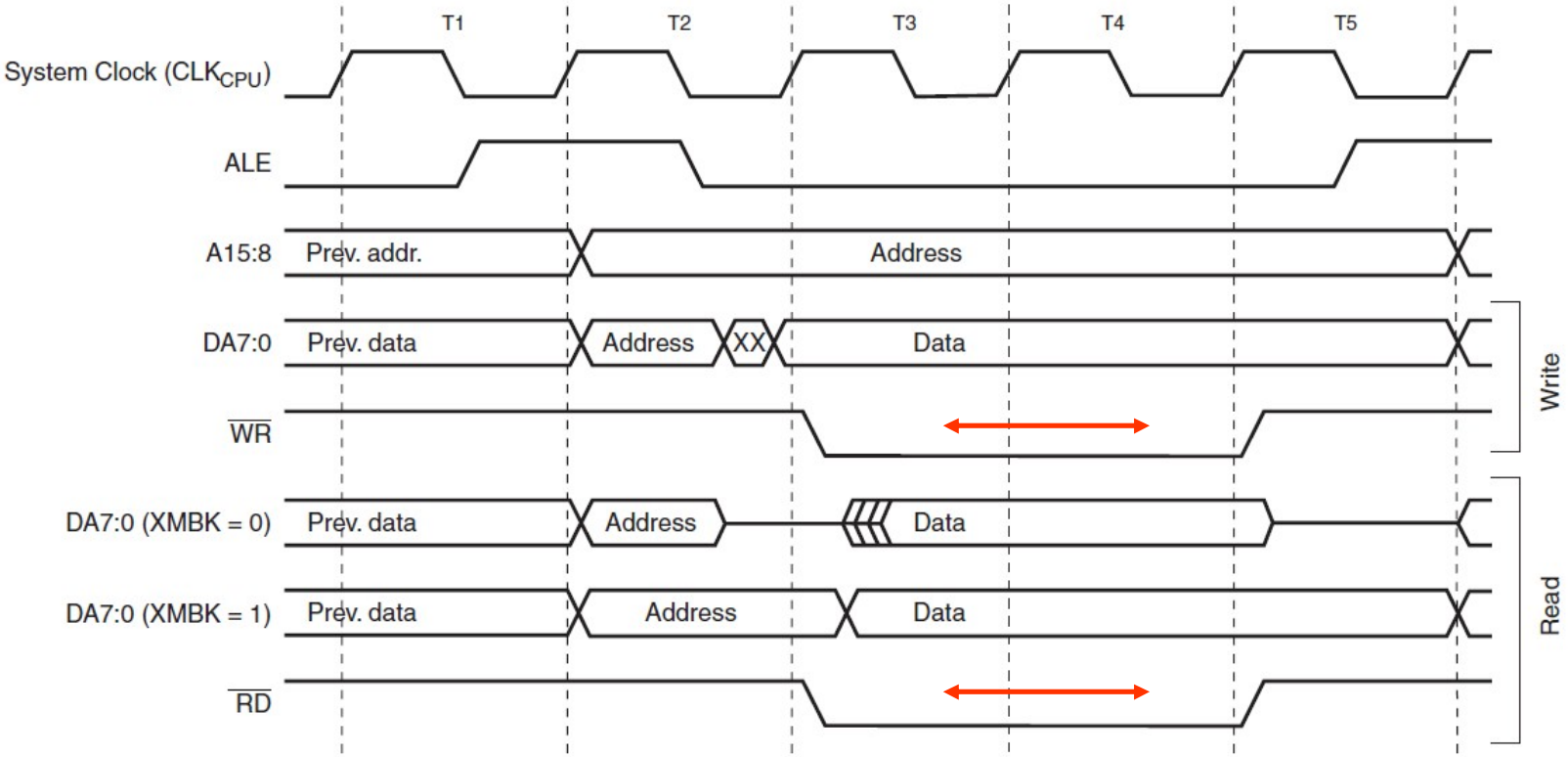


- **AD7:0**: multiplexed low-order address bus and data bus,
- **A15:8**: high order address bus,
- **ALE**: address latch enable,
- **R\D**: read strobe,
- **W\R**: write strobe.

Interfejs pamięci zewnętrznej



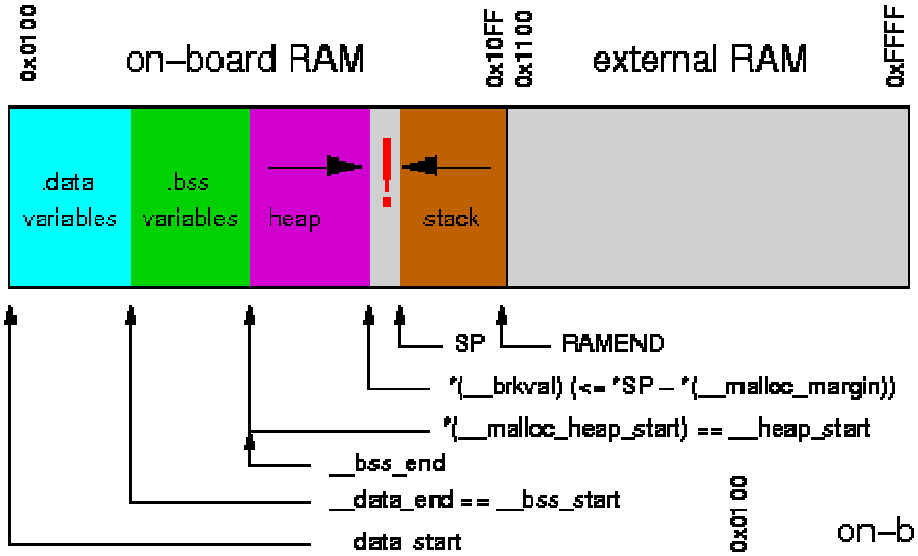
Interfejs pamięci zewnętrznej



Interfejs pamięci zewnętrznej

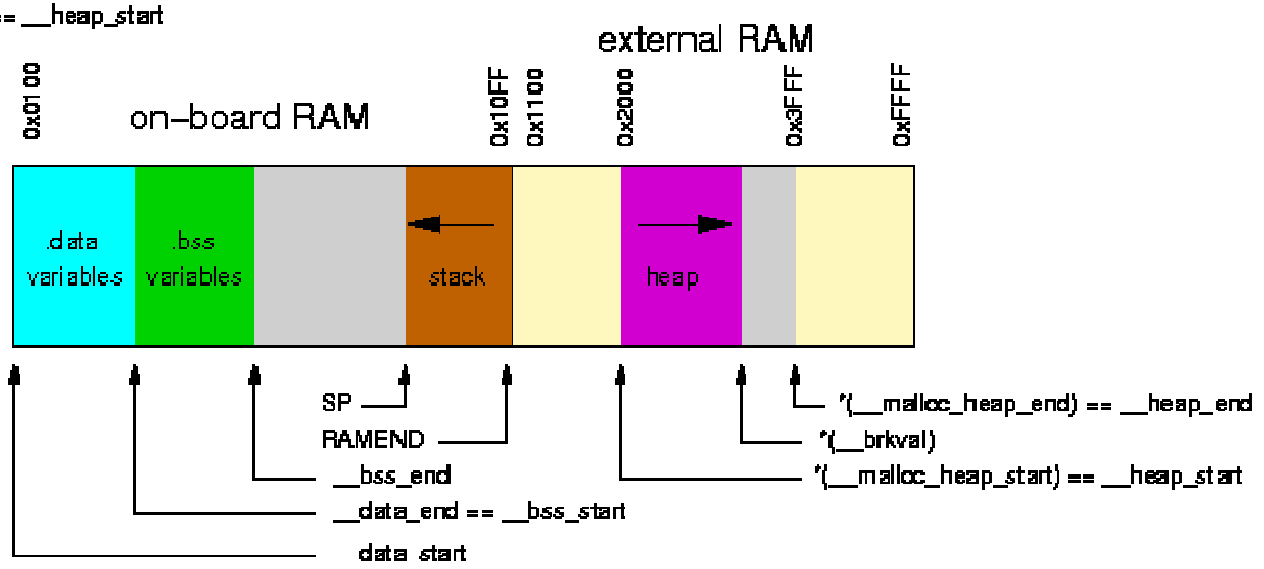
- Włączenie SRE (ang. External SRAM/XMEM Enable) w rej. MCUCR,
- Konfiguracja cykli wait-state w całej przestrzeni pamięci lub w dwu rozdzielnych sektorach,
- Włączenie / wyłączenie obwodów bus-keeper,
- Konfiguracja starszej części szyby adresowej (ilość bitów A15:A8 użytych do adresowania, niewykorzystane linie mogą być używane jako GPIO),

Interfejs pamięci zewnętrznej



<= RAM map of a device with internal RAM

Internal RAM: variables and stack, external RAM: heap



avr-gcc ... -Wl,--defsym=__heap_start=0x802000,--defsym=__heap_end=0x803fff ...

Interfejs pamięci zewnętrznej

```
// Inicjacja pamięci zewnętrznej - robimy to jeszcze zanim program wystartuje
void before_main(void) __attribute__((naked)) __attribute__((section(".init3")));

// Funkcja umieszczona w sekcji .init3
// Stos jest już zainicjowany, rejestr zero_reg jest wyzerowany
// Zmienne jeszcze nie są zainicjowane
void before_main(void) {
   // Włączenie zewnętrznego interfejsu pamięci
   MCUCR |= (1 << SRE);
   // Bity ustawiające podział na bloki oraz wprowadzane cykle opóźnienia
   // w EMCUCR. Domyślne zapewniają brak cykli oczekiwania przy dostępie do
   // zewnętrznej pamięci oraz cały obszar jako jeden segment.
   XMCRA = 0x00;

   // Włączenie podtrzymywania stanu na wyjściach adresowych
   // podtrzymywanie i maskowanie A15
   SFIOR = (1 << XMBK) | (1 << XMM0);

   // Ustawienie A15 na 0
   DDRC = 0x80;
   PORTC &= ~(1 << PC7);
}
```

LDFLAGS += -Wl,--section-start=.exram=0x801100
#define EXMEM __attribute__ ((section (".exram")))

uint8_t lcd_buffer[10 * 10] EXMEM;

Interrupts

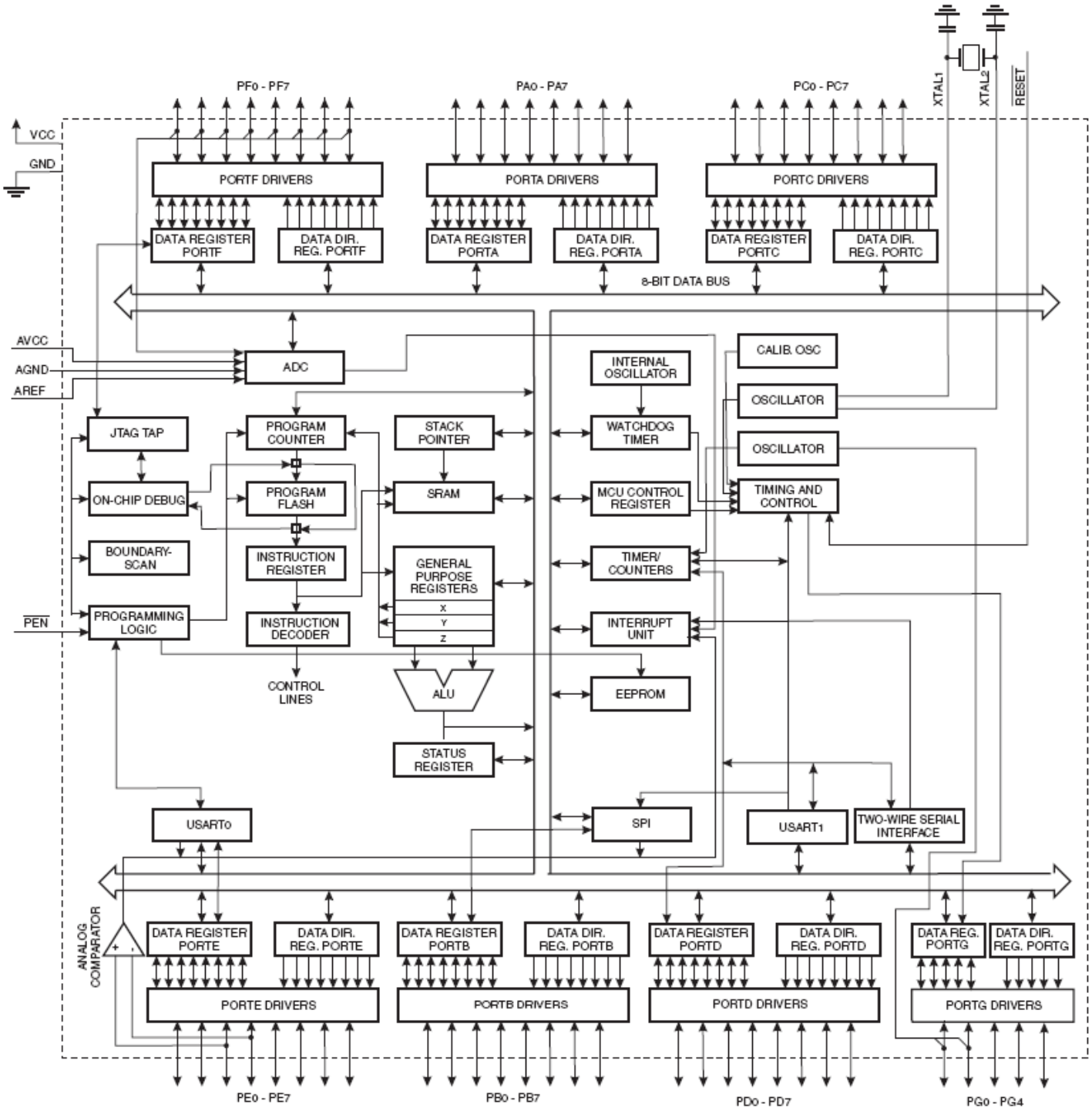
- Kilkanaście źródeł przerwań
- Obsługiwane przez procedury przerwań (ISR’s), których adresy wpisane są do tablicy wektorów przerwań
- Każde przerwanie maskowane jest indywidualnym bitem oraz wszystkie zbiorczo maskowane bitem „I” rejestru SREG
- Przenoszenie tablicy wektorów przerwań w przypadku korzystania z Bootloader’a

Interrupts

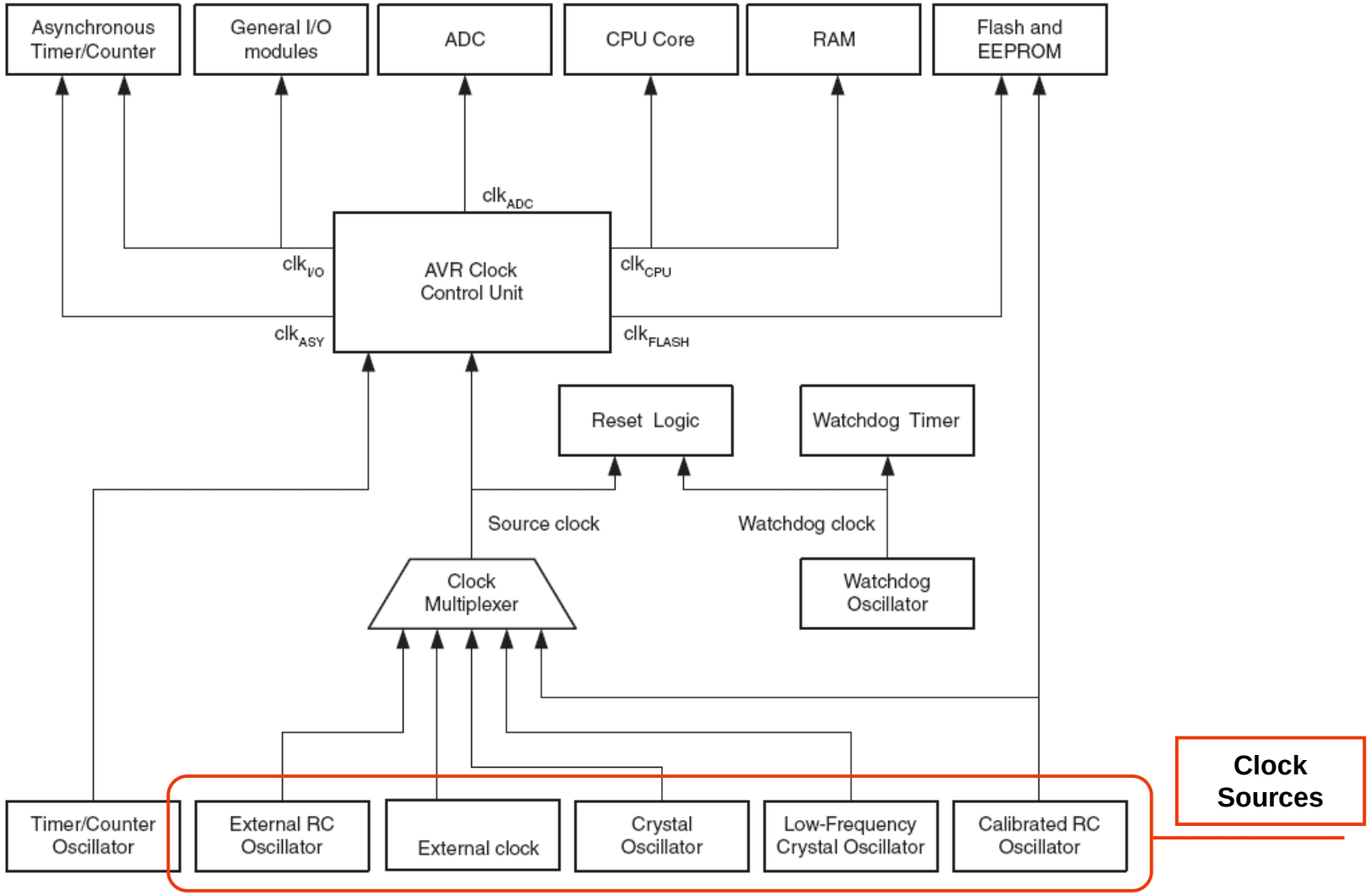
Table 23. Reset and Interrupt Vectors

Vector No.	Program Address[2]	Source	Interrupt Definition
1	$0000[1]	RESET	External Pin, Power-on Reset, Brown-out Reset, Watchdog Reset, and JTAG AVR Reset
2	$0002	INT0	External Interrupt Request 0
3	$0004	INT1	External Interrupt Request 1
4	$0006	INT2	External Interrupt Request 2
5	$0008	INT3	External Interrupt Request 3
6	$000A	INT4	External Interrupt Request 4
7	$000C	INT5	External Interrupt Request 5
8	$000E	INT6	External Interrupt Request 6
9	$0010	INT7	External Interrupt Request 7
10	$0012	TIMER2 COMP	Timer/Counter2 Compare Match
11	$0014	TIMER2 OVF	Timer/Counter2 Overflow
12	$0016	TIMER1 CAPT	Timer/Counter1 Capture Event
13	$0018	TIMER1 COMPA	Timer/Counter1 Compare Match A
14	$001A	TIMER1 COMPB	Timer/Counter1 Compare Match B
15	$001C	TIMER1 OVF	Timer/Counter1 Overflow
16	$001E	TIMER0 COMP	Timer/Counter0 Compare Match
17	$0020	TIMER0 OVF	Timer/Counter0 Overflow
18	$0022	SPI, STC	SPI Serial Transfer Complete
19	$0024	USART0, RX	USART0, Rx Complete
20	$0026	USART0, UDRE	USART0 Data Register Empty
21	$0028	USART0, TX	USART0, Tx Complete
22	$002A	ADC	ADC Conversion Complete
23	$002C	EE READY	EEPROM Ready
24	$002E	ANALOG COMP	Analog Comparator
25	$0030[3]	TIMER1 COMPC	Timer/Countre1 Compare Match C
26	$0032[3]	TIMER3 CAPT	Timer/Counter3 Capture Event
27	$0034[3]	TIMER3 COMPA	Timer/Counter3 Compare Match A
28	$0036[3]	TIMER3 COMPB	Timer/Counter3 Compare Match B
29	$0038[3]	TIMER3 COMPC	Timer/Counter3 Compare Match C
30	$003A[3]	TIMER3 OVF	Timer/Counter3 Overflow
31	$003C[3]	USART1, RX	USART1, Rx Complete
32	$003E[3]	USART1, UDRE	USART1 Data Register Empty
33	$0040[3]	USART1, TX	USART1, Tx Complete
34	$0042[3]	TWI	Two-wire Serial Interface
35	$0044[3]	SPM READY	Store Program Memory Ready

ATmega128(L) Block Diagram



Clock Distribution



Jak wybrać odpowiednią opcję taktowania układu?

Table 119. Fuse Low Byte

Fuse Low Byte	Bit No.	Description	Default Value
BODLEVEL	7	Brown out detector trigger level	1 (unprogrammed)
BODEN	6	Brown out detector enable	1 (unprogrammed, BOD disabled)
SUT1	5	Select start-up time	1 (unprogrammed)(1)
SUT0	4	Select start-up time	0 (programmed)(1)
CKSEL3	3	Select Clock source	0 (programmed)(2)
CKSEL2	2	Select Clock source	0 (programmed)(2)
CKSEL1	1	Select Clock source	0 (programmed)(2)
CKSEL0	0	Select Clock source	1 (unprogrammed)(2)

Power Management And Sleep Modes

	Active Clock Domains					Oscillators		Wake Up Sources					
Sleep Mode	clk_{CPU}	clk_{FLASH}	clk_{IO}	clk_{ADC}	clk_{ASY}	Main Clock Source Enabled	Timer Osc Enabled	INT7:0	TWI Address Match	Timer 0	SPM/ EEPROM Ready	ADC	Other I/O
Idle			X	X	X	X	X(2)	X	X	X	X	X	X
ADC Noise Reduction				X	X	X	X(2)	X(3)	X	X	X	X	
Power-down								X(3)	X				
Power-save					X(2)		X(2)	X(3)	X	X(2)			
Standby(1)						X		X(3)	X				
Extended Standby(1)					X(2)	X	X(2)	X(3)	X	X(2)			

Notes:
1. External Crystal or resonator selected as clock source
2. If AS0 bit in ASSR is set
3. Only INT3:0 or level interrupt INT7:4

Jak długo będzie pracować ATmega128L (@7,3728MHz) zasilona z baterii CR2032 (3V, 220mAh)???
Układ wybudzany jest z trybu Powerdown raz na godzinę na około 1 minutę?

System Control And Reset

The ATmega128 has five sources of reset:

- Power-on Reset. The MCU is reset when the supply voltage is below the Power-on Reset threshold (V_{POT}).
- External Reset. The MCU is reset when a low level is present on the $\overline{\text{RESET}}$ pin for longer than the minimum pulse length.
- Watchdog Reset. The MCU is reset when the Watchdog Timer period expires and the Watchdog is enabled.
- Brown-out Reset. The MCU is reset when the supply voltage V_{CC} is below the Brown-out Reset threshold (V_{BOT}) and the Brown-out Detector is enabled.
- JTAG AVR Reset. The MCU is reset as long as there is a logic one in the Reset Register, one of the scan chains of the JTAG system. Refer to the section "IEEE 1149.1 (JTAG) Boundary-scan" on page 252 for details.

System Control And Reset

Figure 23. MCU Start-up, $\overline{\text{RESET}}$ Tied to V_{CC}.

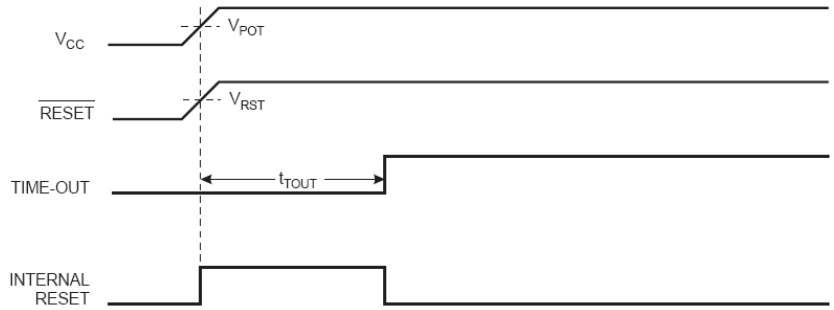


Figure 24. MCU Start-up, $\overline{\text{RESET}}$ Extended Externally

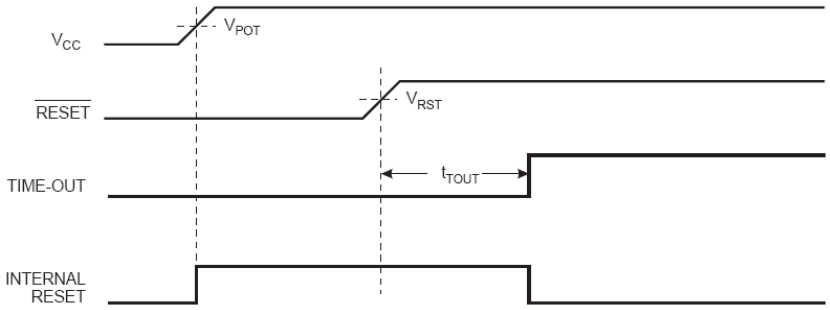


Figure 25. External Reset During Operation

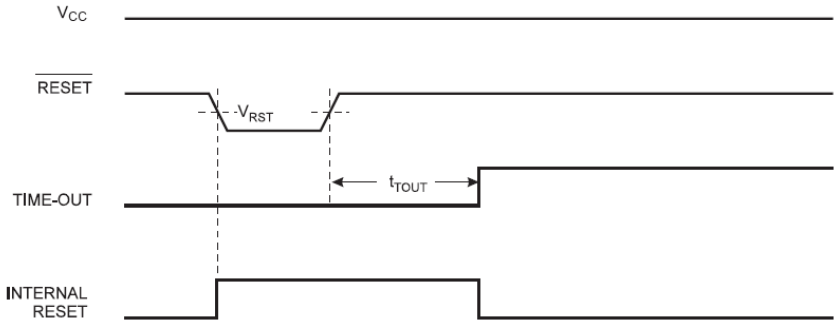
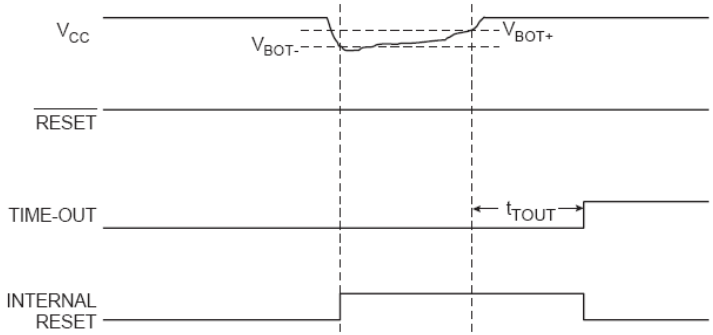


Figure 26. Brown-out Reset During Operation



System Control And Reset

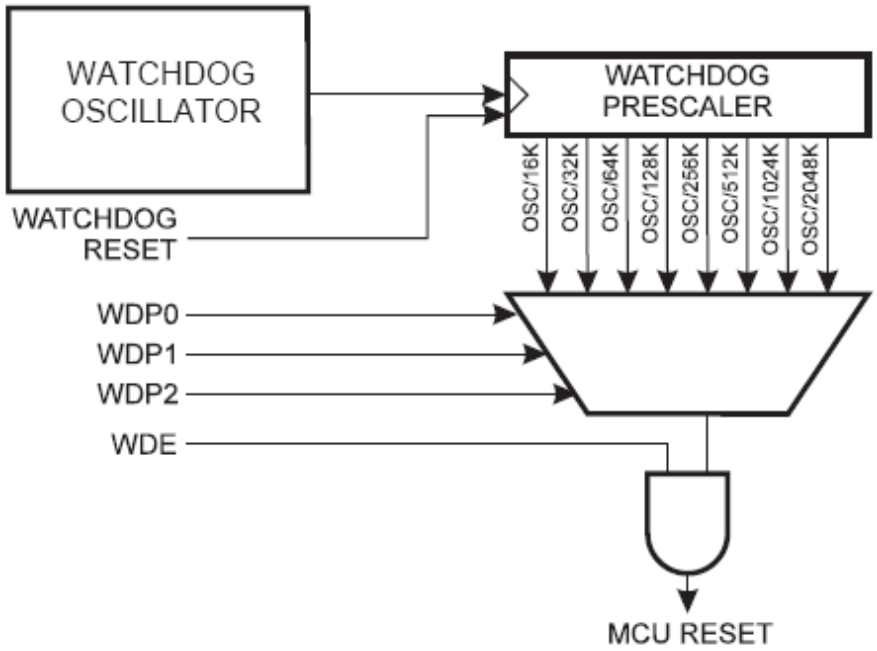
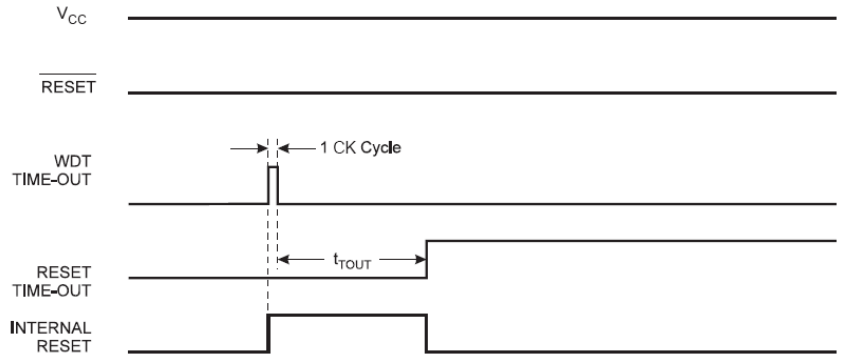


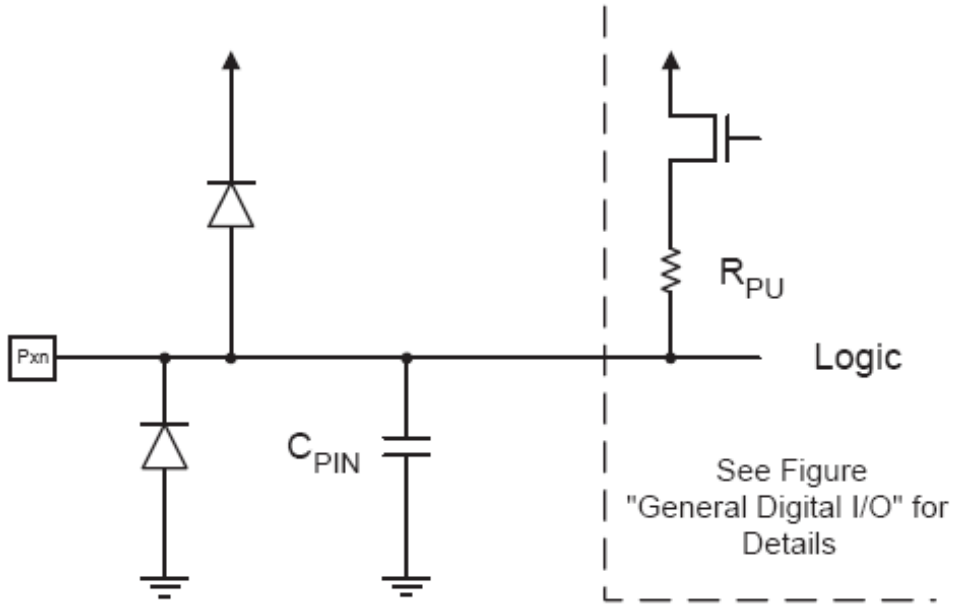
Figure 27. Watchdog Reset During Operation



Porty GPIO

- Sześć 8-bitowych portów oznaczonych literami A .. F
- Jeden 5-bitowy port oznaczony literą G
- Wszystkie porty dwukierunkowe, z możliwością indywidualnej zmiany kierunku dowolnej linii portu

Figure 29. I/O Pin Equivalent Schematic



Porty GPIO

- Dostęp poprzez zestaw rejestrów dla każdego z portów (tu PORTA):

Port A Data Register – PORTA

Bit	7	6	5	4	3	2	1	0	
	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	PORTA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port A Data Direction Register – DDRA

Bit	7	6	5	4	3	2	1	0	
	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port A Input Pins Address – PINA

Bit	7	6	5	4	3	2	1	0	
	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	PINA
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

Porty GPIO - konfiguracja

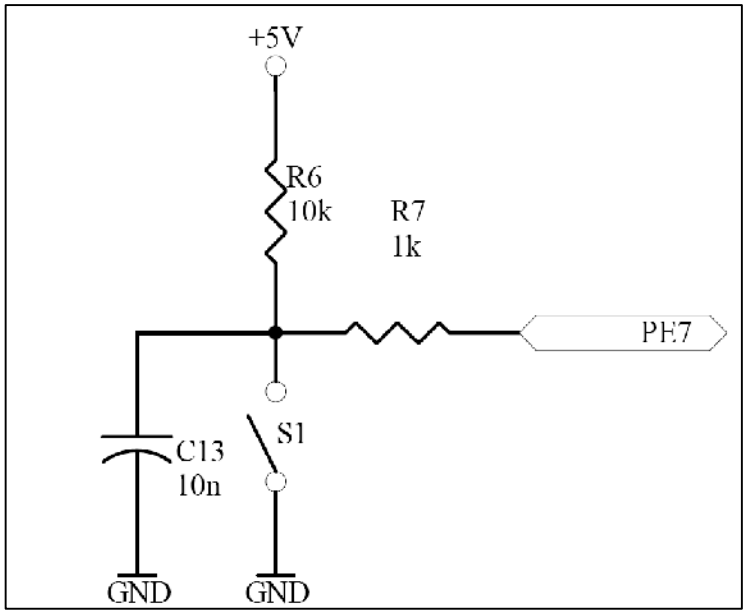
PUD – *Pull Up Disable*:

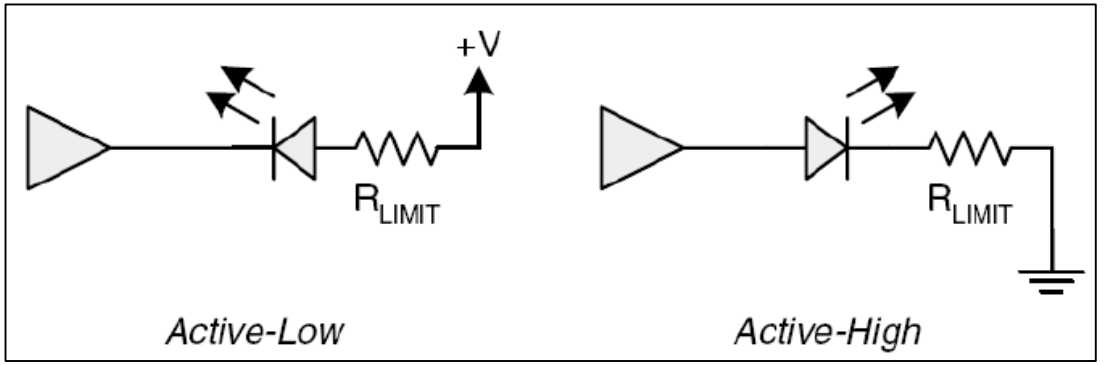
1 – wyłączone ‘rezystory pull-up’

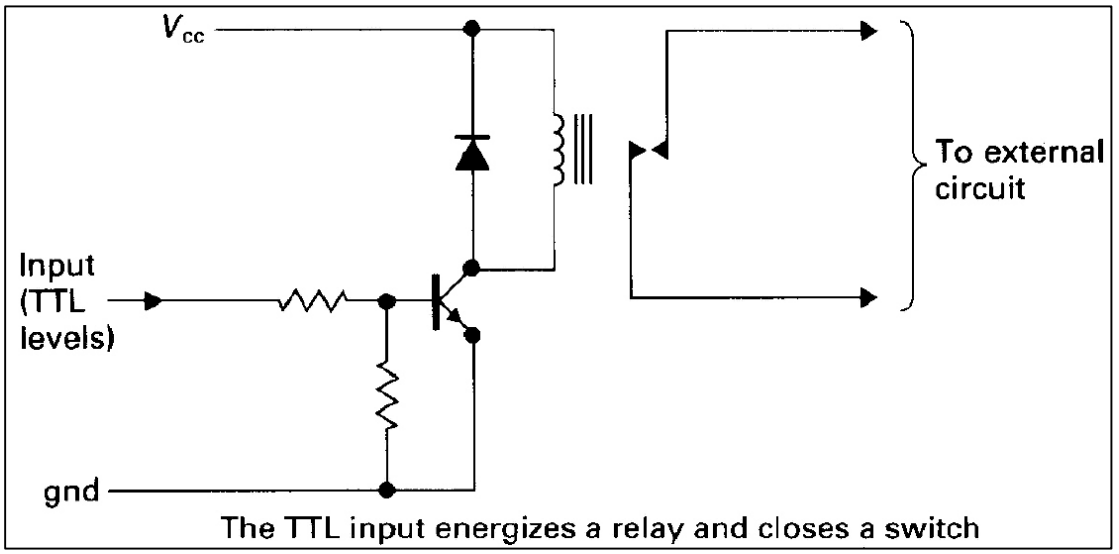
Table 25. Port Pin Configurations

DDxn	PORTxn	PUD (in SFIOR)	I/O	Pull-up	Comment
0	0	X	Input	No	Tri-state (Hi-Z)
0	1	0	Input	Yes	Pxn will source current if ext. pulled low.
0	1	1	Input	No	Tri-state (Hi-Z)
1	0	X	Output	No	Output Low (Sink)
1	1	X	Output	No	Output High (Source)

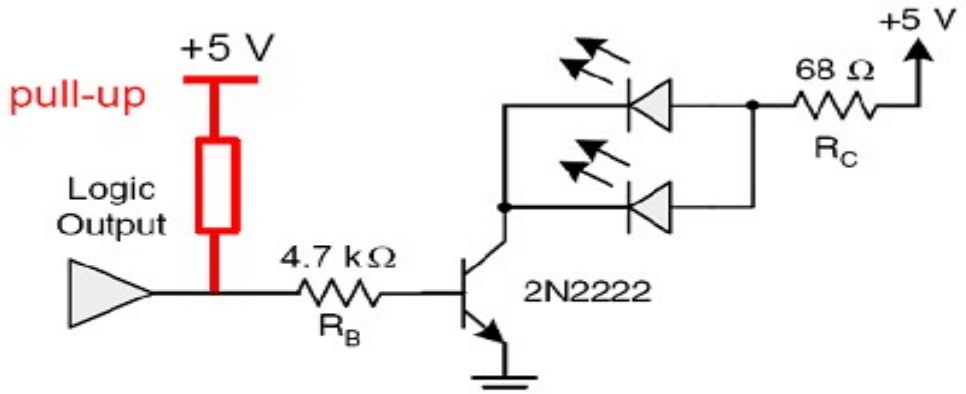
Porty GPIO - wykorzystanie



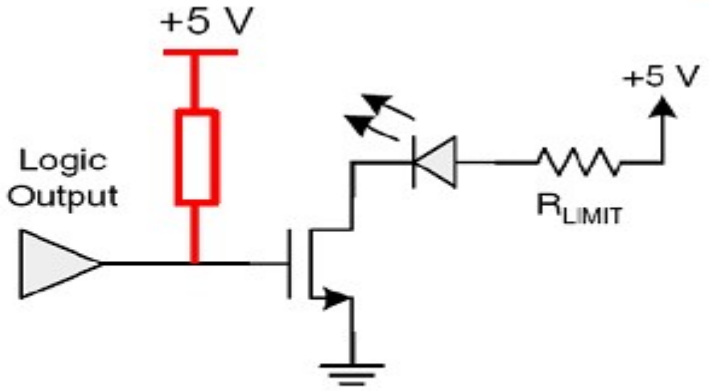




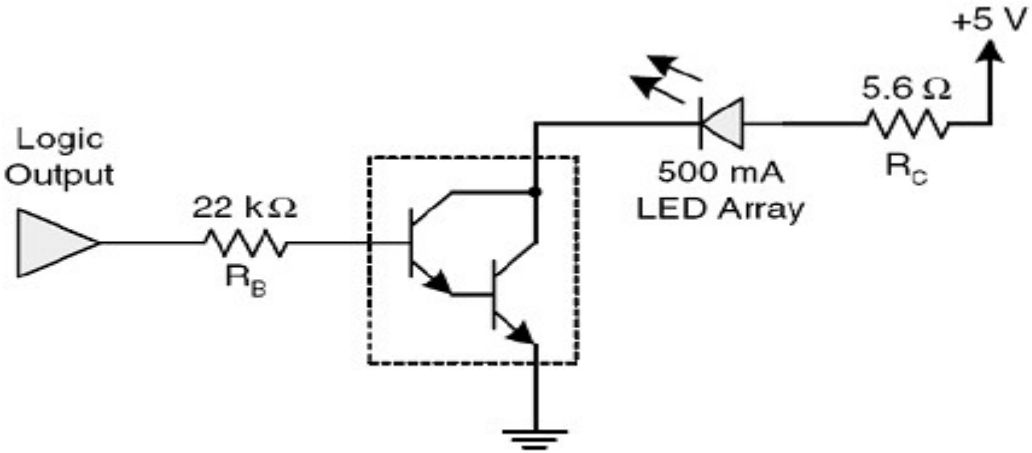
Porty GPIO - wykorzystanie



Tranzystor bipolarny n-p-n

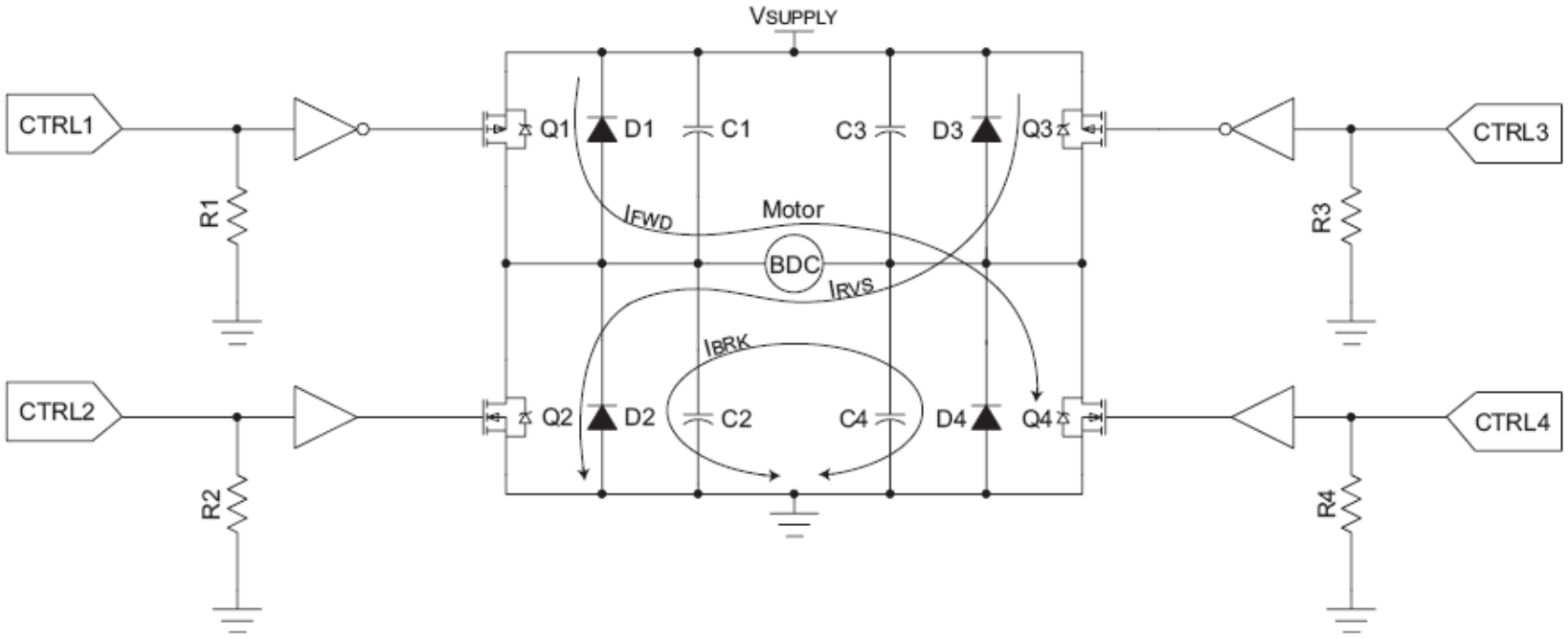


Tranzystor NMOS



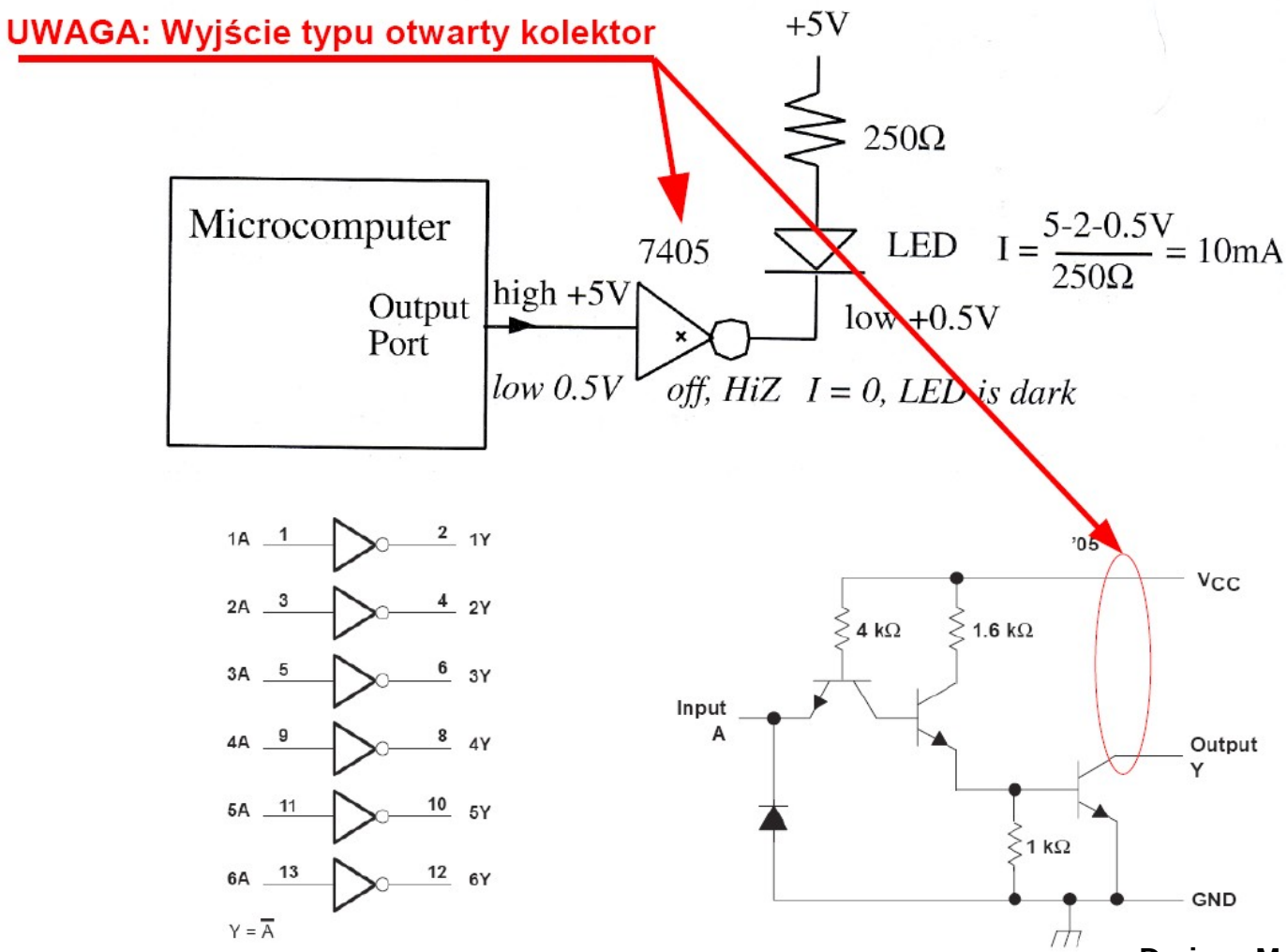
Tranzystor w układzie Darlingtona

Porty GPIO - wykorzystanie



	Q1 (CTRL1)	Q2 (CTRL2)	Q3 (CTRL3)	Q4 (CTRL4)
Forward	on	off	off	on
Reverse	off	on	on	off
Coast	off	off	off	off
Brake	off	on	off	on

Porty GPIO - wykorzystanie



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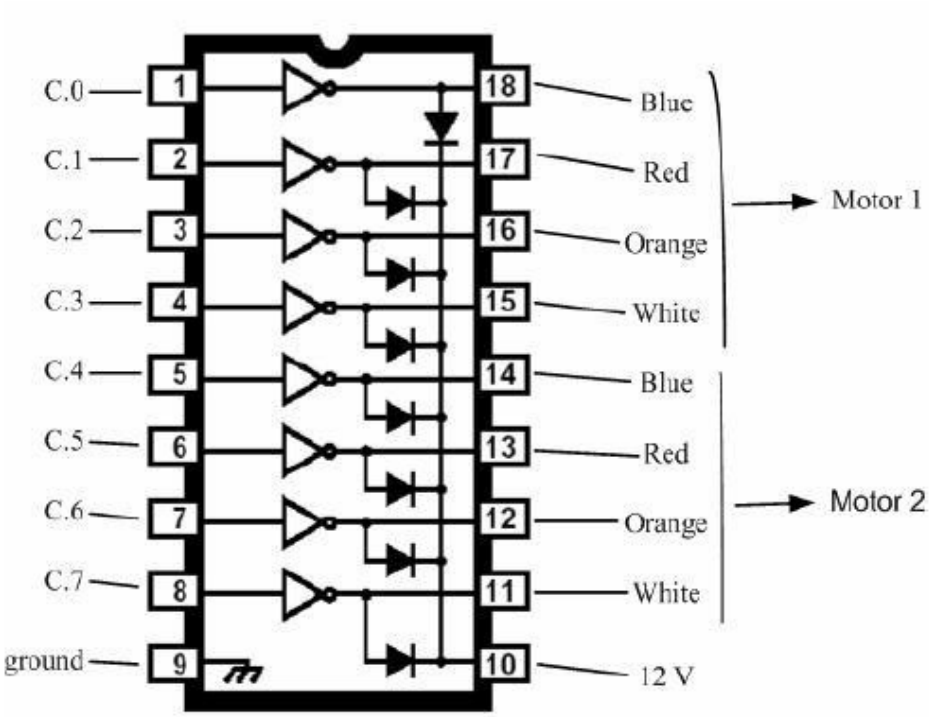
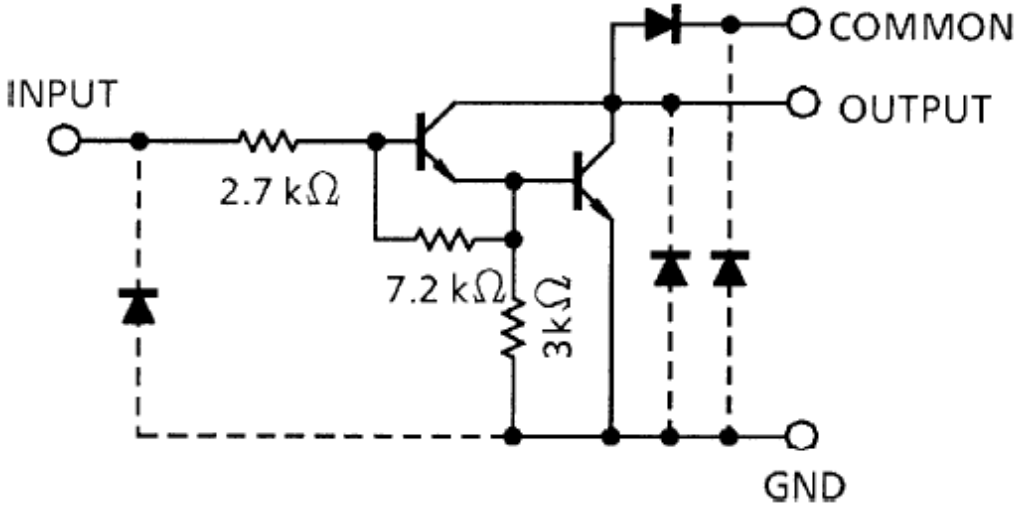
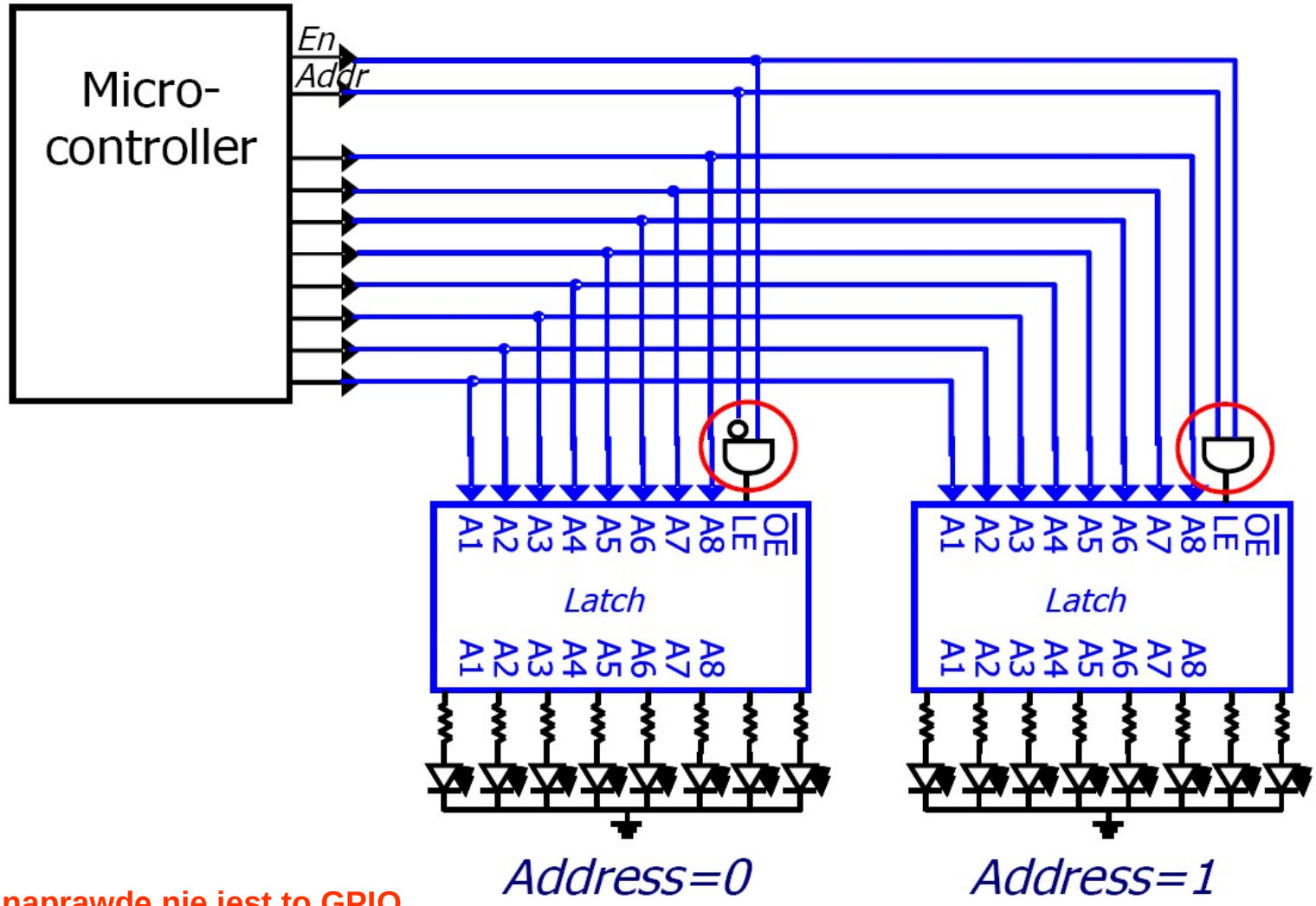
Porty GPIO - wykorzystanie

ULN2803 – proste zwiększenie wydajności prądowej





Dodatkowe porty GPIO



Wada – tak naprawdę nie jest to GPIO…

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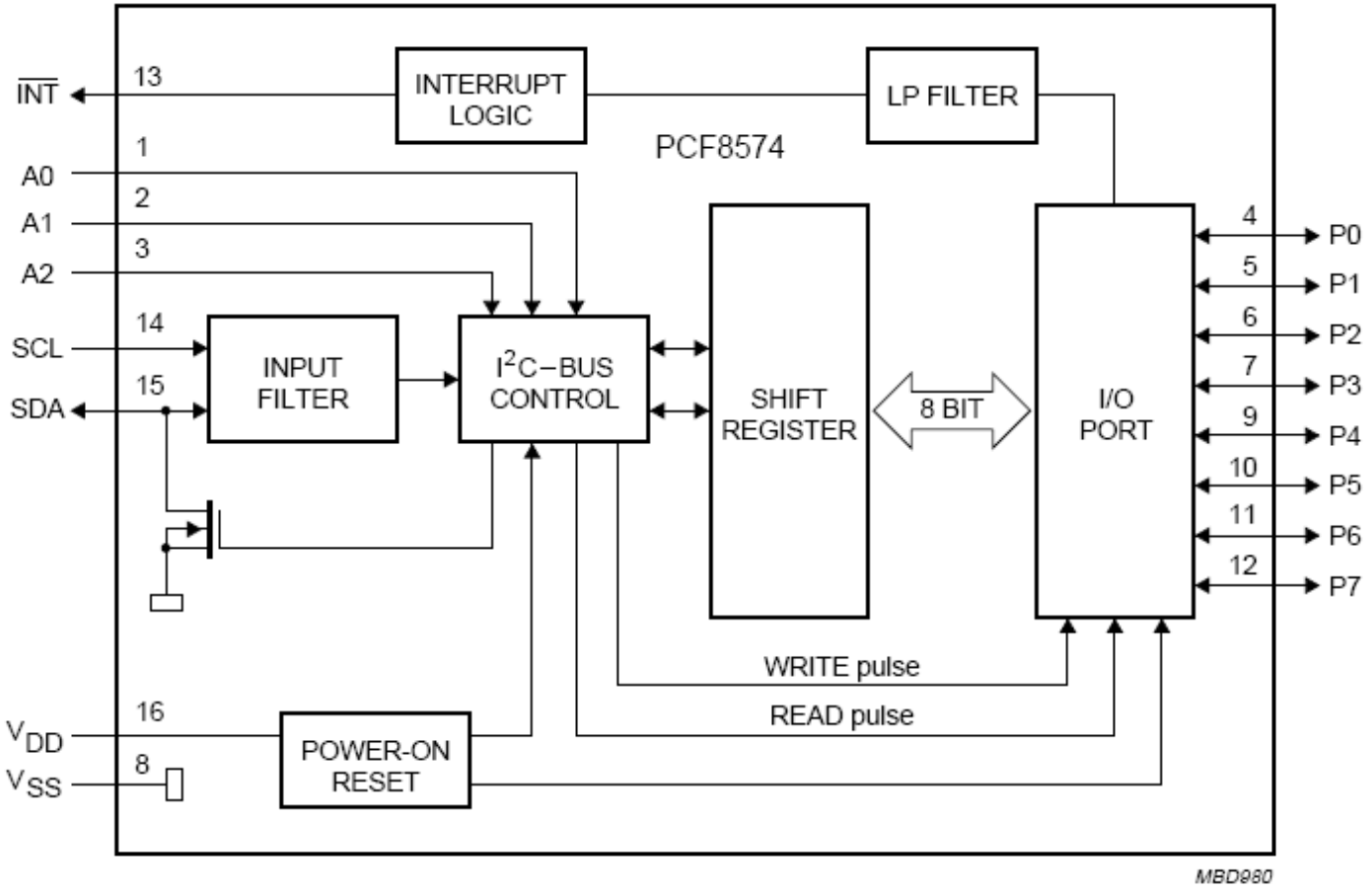
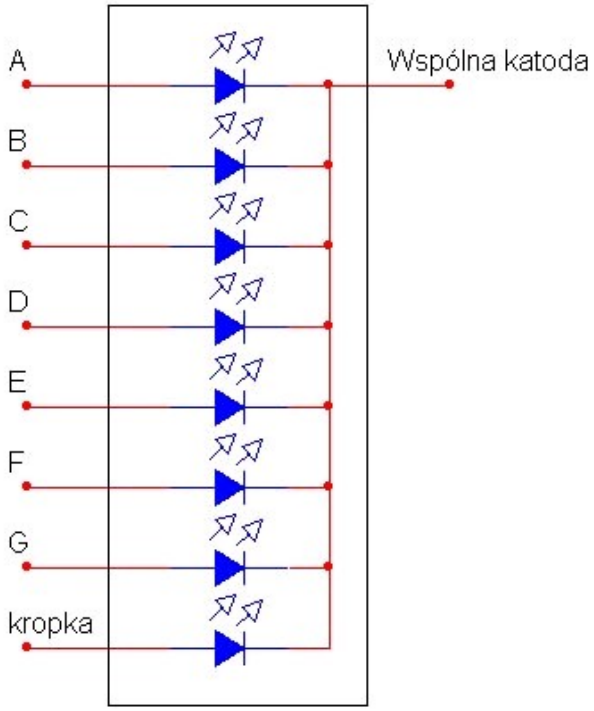
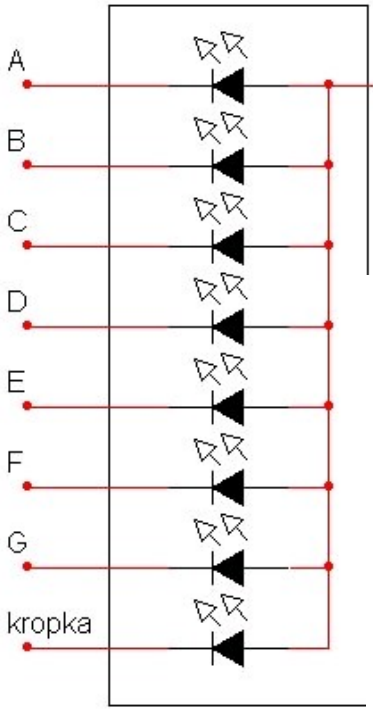
Dodatkowe porty GPIO

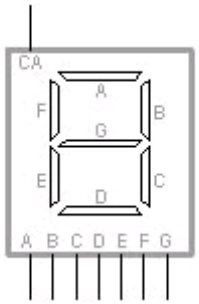
PCF8574 – Remote 8-bit I/O expander for I2C bus

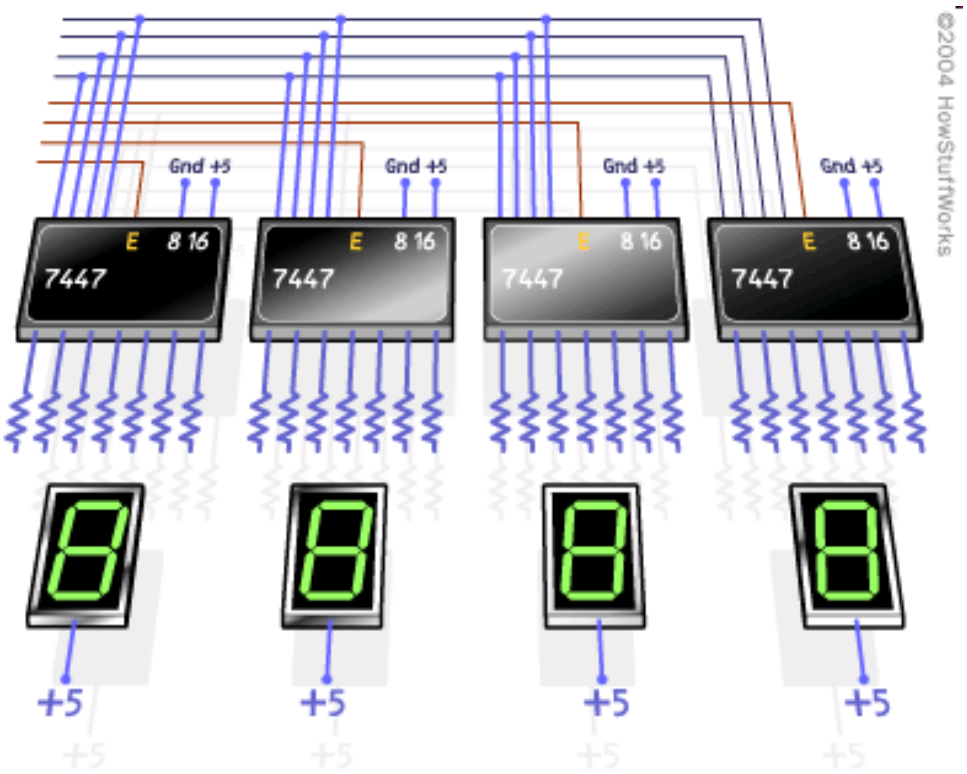


Wyświetlacze 7-segmentowe

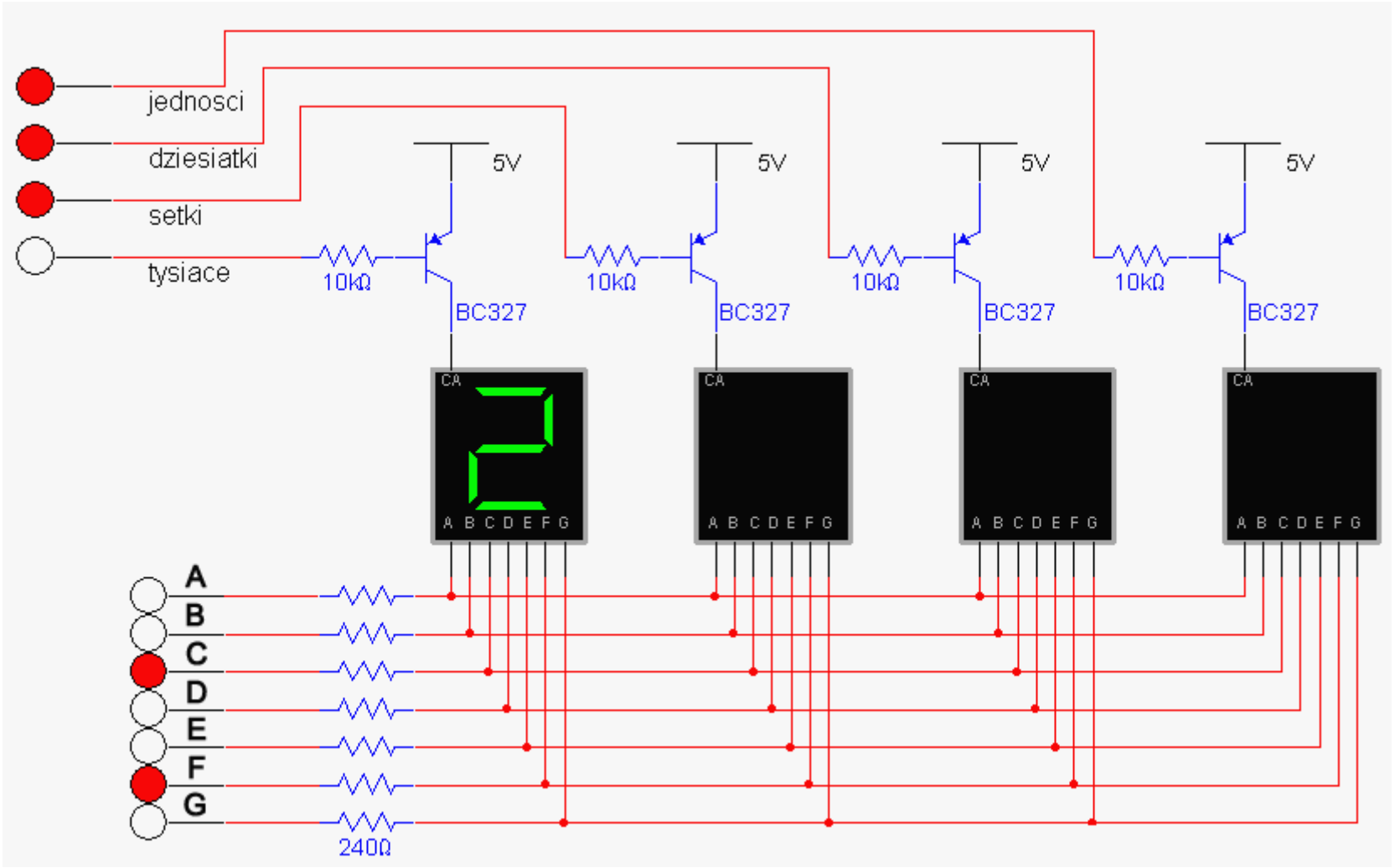








Wyświetlacze 7-segmentowe



Wyświetlacze 7-segmentowe

STP08DP05 – Low voltage 8-bit constant current LED sink with full outputs error detection